I²C Communication, 500mA Single Cell Li-Ion Battery Charger with Power Path Management， 1mA Termination and <1uA Battery Leakage

DESCRIPTION

The ETA4662 is a single cell battery charger with power path management function for Li-Ion and Li-Polymer battery. It features pre-charging, fast charging (CC) and constant voltage (CV) charging, end-of charging termination, and auto-recharge, and built-in safe-timer preventing from being over-charged or host running out of control.

The power path management function features a low dropout regulator from the input to the system and a low R_{DSON} switch from battery to the system, so it separates the charging current from the system load. This function prioritizes the battery and the system, ensuring the continuous power supply to the system.

Parameters and functions are programmed or selected through an I²C compatible serial interface, such as input current limit, charging current, battery regulation voltage, safety timer, battery UVLO. It also features a safe watchdog protection.

The ETA4662 is available in FCQFN-9L package.

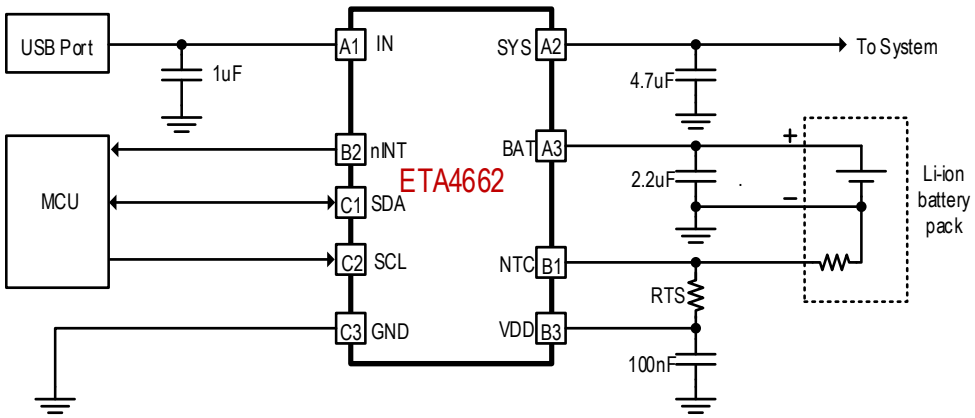
FEATURES

- Fully Autonomous Charger for Single Cell Li-Ion and Li-Polymer Battery
- 21V Maximum Input Voltage Rating with Over-Voltage Protection
- I²C Interface for Setting Charging Parameters and Status Reporting
- Fully Integrated Power Switch and No External Blocking Diode Required
- Battery Temperature Monitor and Programmable Timer
- Battery or PCB Over-Temperature Protection
- System Reset Function
- Battery Disconnection Function
- Thermal Limiting Regulation on Chip
- FCQFN-9L 1.75x1.75mm

APPLICATIONS

- Wearable Devices
- Smart Watches
- IoT Gadgets
- Smart Handheld Devices

TYPICAL APPLICATION

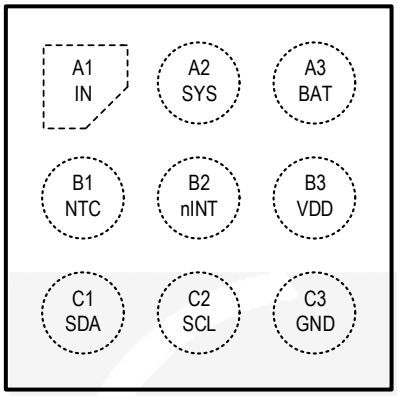


ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA4662FQFJ	FCQFN	SJYW	3000

PIN CONFIGURATION

Top View



FCQFN1.75x1.75-9L

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

IN Pin Voltage to GND.....-0.3V to 28V
V_{IN} to GND Discharge Current.....5mA
V_{SYS} to GND Voltage..... -0.3V to 5.5V
BAT pin Voltage to GND.....-1V to 6V
All Other Pins Voltage to GND.....-0.3V to 6V
V_{SYS}, V_{BAT} to Ground Current.....Internally Limited
Operating Temperature Range.....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C

Thermal Resistance	θ_{JC}	θ_{JA}	
FCQFN1.75x1.75-9L	12	114	°C/W

Lead Temperature (Soldering 10 secs).....260°C
ESD HBM (Human Body Mode) 4KV
ESD CDM (Charged Device Mode).....1KV

ELECTRICAL CHARACTERISTICS

(V_{BAT} = 3.6V, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	TESTCONDITIONS	MIN	TYP	MAX	UNIT
INPUT AND BATTERY CONDITION					
Input Under Voltage Lock Out Threshold	V_{IN} Falling	3.63	3.73	3.83	V
V_{IN_UVLO} Hysteresis	V_{IN} Rising		170		mV
Input Over Voltage Protection Threshold	V_{IN} Rising	5.85	6	6.15	V
V_{IN_OVP} Hysteresis	V_{IN} Falling		350		mV
Input Clamp Voltage	Test for having 1mA clamp current.	20			V
Input Discharge Current	V_{IN} = 21V		5		mA
V_{HDRM}(Sleep-Mode Entry Threshold, V_{IN} – V_{BAT})	V_{IN} Falling vs. V_{BAT}		85		mV
Sleep-Mode Exit Hysteresis	V_{IN} Rising vs. V_{BAT}	100	130	160	mV
BAT Input Voltage Range				5	V
Input Detection Deglitch Time	For either under-voltage or over-voltage		250		µs
Input Power Detection Time	Time before reporting Power ON or OFF	50	75	100	ms

PARAMETER	TESTCONDITIONS		MIN	TYP	MAX	UNIT
Battery Under Voltage Lockout Threshold (Falling)	V_{BAT_UVLO}[2:0] = 000		2.3	2.4	2.5	V
	V_{BAT_UVLO}[2:0] = 100		2.66	2.76	2.86	V
	V_{BAT_UVLO}[2:0] = 111		2.93	3.03	3.13	V
V_{BAT_UVLO} Hysteresis	V_{BAT} Falling, V_{BAT_UVLO}=2.76V(Default)			210		mV
Battery Over Voltage Protection Threshold	V_{BAT} Rising, higher than V_{TERM}			130		mV
V_{BAT_OVP} Hysteresis	V_{BAT} Falling			70		mV
Battery Over-Voltage Discharge Current				5		μA
SUPPLY CURRENT CONDITION						
Input Quiescent Current	V_{IN}=5.5V, I_{SYS}=0A, I_{CHG}=0A, EN_HIZ =0	CEB=0		250		μA
		CEB=1		200		μA
Input Suspend Current	V_{IN}=5.5V,V_{BAT}=4.3V,EN_HIZ =1			70		μA
Battery Quiescent Current	V_{IN}=5V, CEB=0, V_{BAT}=4.3V, I_{SYS}=0A, Charge done			12		μA
	V_{IN}=GND, CEB=1, V_{DD_GATE}=1, BFET_DIS=0,SWITCH_MODE=0, V_{BAT}=4.35V, I_{SYS}=0A ,disable driving to external NTC circuit			5		μA
	V_{IN}=GND,SWITCH_MODE=1, V_{BAT}=4.35V, I_{SYS}=0A ,disable driving to external NTC circuit			1		μA
	V_{IN}=GND, CEB=1, I_{SYS}=0A V_{BAT}=4.35V,Enable PCB OTP function, not include the external NTC bias			8		μA
	V_{IN}=GND,CEB=1,V_{BAT}=4.35V,I_{SYS}=0A, Enable PCB OTP function and Watchdog, not include the external NTC bias			22		μA
	V_{BAT}=4.5V, V_{IN}=V_{SYS}=0V,FET_DIS=1, shipping mode				1	μA
POWER PATH MANAGEMENT						
Regulated System Output Voltage Accuracy	V_{IN} = 5.5V, R_{SYS}=100Ω	V_{SYSREG}[3:0]=0000	4.15	4.2	4.25	V
		V_{SYSREG}[3:0]=1001	4.60	4.65	4.70	
		V_{SYSREG}[3:0]=1111	4.90	4.95	5.00	

PARAMETER	TESTCONDITIONS	MIN	TYP	MAX	UNIT
System Over Voltage Protection to Discharger	V_{SYS} Rising, As Percentage of V_{SYS_REG}		10		%
V_{SYS_OVP} Hysteresis	V_{SYS} Falling, As Percentage of V_{SYS_REG}		5		%
V_{SYS} Discharge Resistance	V_{SYS} > V_{SYS_OVP}		400		Ω
Input Minimum Voltage Regulation	VINDPM[3:0]=0000	3.78	3.88	3.98	V
	VINDPM[3:0]=1001	4.50	4.60	4.70	
	VINDPM[3:0]=1111	4.98	5.08	5.18	
Input Current Limiting	IN_ILIM[3:0]=0000 for I_{IN_LIM}=50mA	30	40	50	mA
	IN_ILIM[3:0]=0011 for I_{IN_LIM} =140mA	125	135	155	
	IN_ILIM[3:0]=1001 for I_{IN_LIM} =320mA	200	320	340	
	IN_ILIM[3:0]=1111 for I_{INDPM}=500mA	440	470	500	
IN to SYS Switch On Resistance	V_{IN}=4.5V, I_{SYS}=100mA		270		mΩ
BATFET On Resistance	V_{IN} < 2V, V_{BAT}=3.5V, I_{SYS}=100mA		170		mΩ
Battery Discharge Current Limit	IDISCHG[3:0] = 0001		400		mA
	IDISCHG[3:0] = 1001		2000		
	IDISCHG[3:0] = 1111		3200		
Discharge Short Circuit Limit			3.7		A
Maximum V_{IN} Current to Shutoff	V_{SYS} falling below V_{HSHORT}		360		mA
V_{HSHORT}(V_{SYS} Short Detection Threshold)			1.5		V
Delay Before Over Current Cut			60		μs
Delay Before Retry After Cut			800		μs
Ideal Diode Forward Voltage in Supplement Mode	10mA Discharge Current		20		mV
DYNAMIC POWER MANAGEMENT AND BATTERY SUPPLEMENT					
SYS Drop For Lowering Charging			90		mV
IN Drop For Lowering Charging			160		mV
V_{SYS} - V_{BAT} Drop For Supplement			30		mV
V_{SYS} - V_{BAT} Regulation in Supplement			22.5		mV
V_{SYS} - V_{BAT} Drop For Exit Supplement			20		mV
SHIPPING MODE AND BATFET RESET					
Enter Shipping Mode Deglitch Time	FET_DIS is set from 0 to 1, EN_SHIPPING_DGL[1:0]=00		1		s
Exit Shipping Mode by Push Button	nINT is pulled low		2		s

PARAMETER	TESTCONDITIONS	MIN	TYP	MAX	UNIT
Exit Shipping Mode by V_{IN} Plug-in			68		ms
Reset by nINT	$t_{RST\_DGL[1:0]}$ = 00		8		s
	$t_{RST\_DGL[1:0]}$ = 10		16		
BATFET Off Lasting Time	$t_{RST\_DGL[0]}$ = 0		2		s
	$t_{RST\_DGL[0]}$ = 1		4		
BATTERY CHARGER					
Battery Charge Termination Voltage Regulation (Aging and pre-condition drift included in 0°C~50°C)	VTERM[5:0] = 000000	3.582	3.60	3.618	V
	VTERM[5:0] = 101000	4.179	4.200	4.221	
	VTERM[5:0] = 110010	4.358	4.380	4.402	
	VTERM[5:0] = 111110	4.522	4.545	4.568	
Fast Charge Current	ICHRG[5:0]=000000		8		mA
	ICHRG[5:0]=001011	91	96	101	
	ICHRG[5:0]=100000	251	264	277	
	ICHRG[5:0]=111000	433	456	479	
Pre-Charge Current	I_{PRE} = I_{TERM}	1		31	mA
Charge Termination Current Threshold	ITERM[3:0]=0000		1		mA
	ITERM[3:0]=0001	2.7	3	3.3	
	ITERM[3:0]=0101	10	11	12	
	ITERM[3:0]=1111	28	31	34	
Precondition to Fast Charge Threshold	Rising, VPRECOND = 1	2.9	3.0	3.1	V
Precondition to Fast Charge Hysteresis	Falling		90		mV
Auto Recharge Voltage Threshold	Below V_{TERM}, VRECHG = 0	70	100	130	mV
	Below V_{TERM}, VRECHG = 1	160	200	240	
Termination Deglitch Time			200		ms
Battery Auto-Recharge Deglitch Time			200		ms
Fast Charge Safety Timer	CHG_TMR [1:0]=01, EN_TIMER = 1		5		hrs
THERMAL PROTECTION					
Junction Temperature Regulation Range	I^2C programmable range	60		120	˚C
Junction Temperature Regulation	TJ_REG[1:0] =11 for Thermal Regulation=120°C		120		˚C
Thermal Shutdown Threshold			150		˚C
Thermal Shutdown Hysteresis			20		˚C

PARAMETER	TESTCONDITIONS	MIN	TYP	MAX	UNIT
NTC Pin Output Current	V_{NTC} = 3V	-100	0	100	nA
NTC Cold Temperature Threshold	V_{NTC} Rising , As percentage of V_{LDO}	63	65	67	%
NTC Cold Temperature Hysteresis	V_{NTC} Falling , As percentage of V_{LDO}		30		mV
NTC Hot Temperature Threshold	V_{NTC} Falling , As percentage of V_{LDO}	31	33	35	%
NTC Hot Temperature Hysteresis	V_{NTC} Rising , As percentage of V_{LDO}		70		mV
NTC Hot Temperature Threshold for PCB OTP	V_{NTC} Falling , As percentage of V_{LDO}	30	32	34	%
NTC Hot Temperature Hysteresis for PCB OTP	V_{NTC} Rising , As percentage of V_{LDO}		85		mV
LOGIC IO PIN SPECIFICATION, nINT, SCL, SDA					
Input Low Logic Voltage Threshold	Falling			0.4	V
Input High Logic Voltage Threshold	Rising	1.3			V
Output Low Level	I_{SINK} = 5mA			0.4	V
I²C SPECIFICATION					
I²C Clock Frequency				400	KHz
WATCHDOG					
Watchdog Timer	WATCHDOG[1:0]=11		160		s

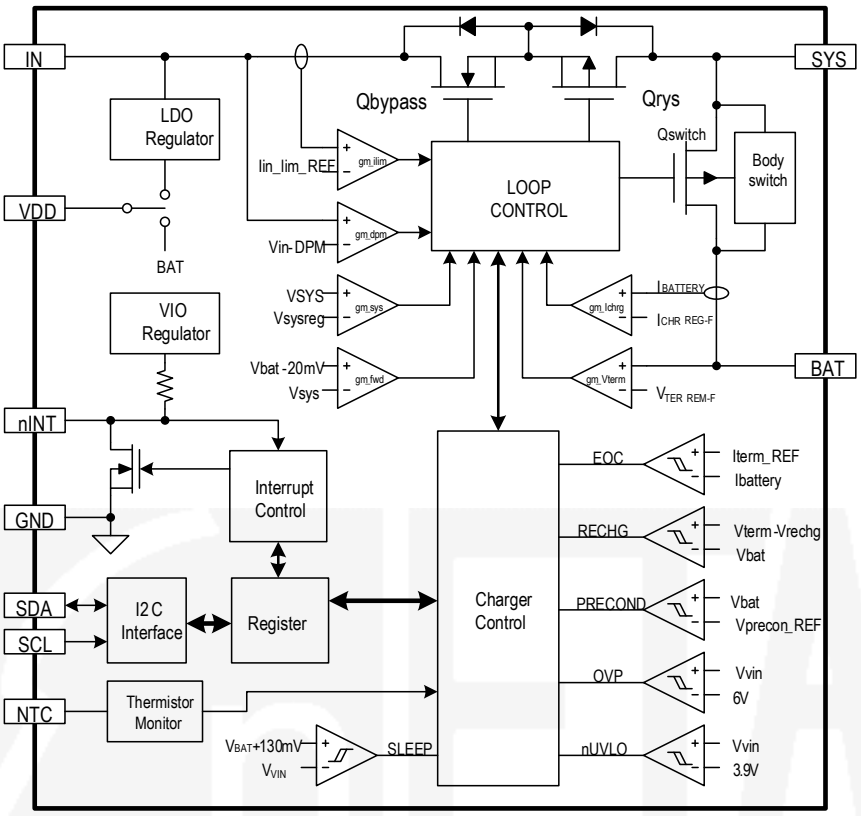
NOTE: For lowering the bias current in the chip, and also to avoid biasing external circuit with output of nINT, the logic high level of the nINT should be a buffered level of an internal reference in range of 1.8~2.5V, at a roughly regulated voltage level.

PIN DESCRIPTION

PIN #	PIN NAME	TYPE	DESCRIPTION
A1	IN	P	Input Power Pin. Place a ceramic capacitor from IN pin to GND as close as possible to this device.
A2	SYS	P	System Power Supply. Place a ceramic capacitor from SYS pin to GND as close as possible to this device.
A3	BAT	P	Battery Pin. Place a ceramic capacitor from BAT pin to GND as close as possible to IC.
B1	NTC	AIO	Battery Temperature Qualification Input Pin. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from VDD to NTC to GND. Charge suspends when either NTC pin is out of range. When NTC pin is not used, connect a 10-kΩ resistor from VDD to NTC and connect a 10-kΩ resistor from NTC to GND. Or NTC can be used like charge disable input pin.
B2	nINT	AIO	Interrupt Output and Battery FET Reset Input pin. The nINT pin sends charging status and fault notification to the host. This pin is also used to reset the system from the battery. Refer to "*Interrupt to Host (nINT)*" and "*Battery Disconnection Function*" sections for detail information.
B3	VDD	P	Internal Control Power Supply Pin. Connect a 0.1μF ceramic cap from this pin to GND.
C1	SDA	DIO	I²C Interface Data. Connect SDA pin to the logic rail through a 10kΩ resistor.
C2	SCL	DI	I²C Interface Clock. Connect SCL pin to the logic rail through a 10kΩresistor.
C3	GND	P	Ground Pin

NOTE: AIO = Analog Input /Output; DI = Digital Input; DO = Digital Output; DIO = Digital Input /Output; P = Power.

FUNCTIONAL BLOCK DIAGRAM

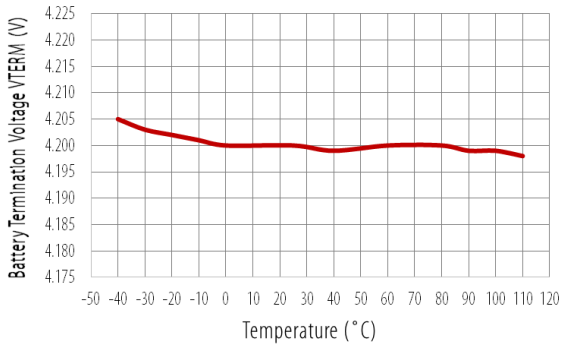


TYPICAL PERFORMANCE CHARACTERISTICS

(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

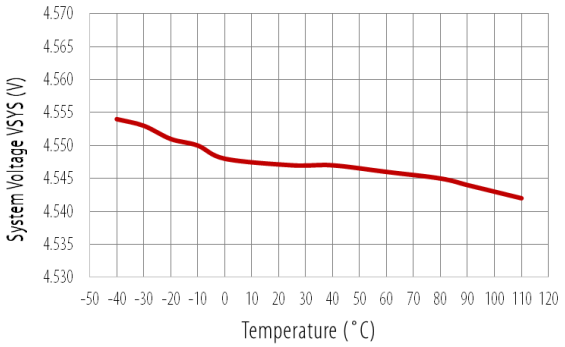
Battery Regulation Voltage vs. Temperature

VBAT_REG[5:0] =101000, I_{BAT} = 10mA



System Regulation Voltage vs. Temperature

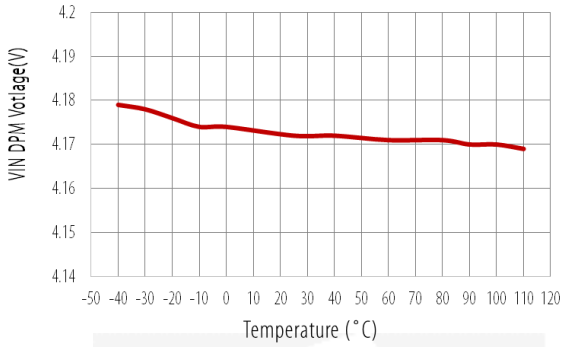
VSYS_REG[3:0] =0111, I_{VSYS} = 10mA



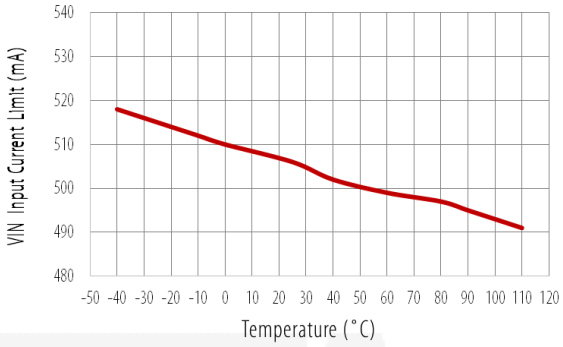
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

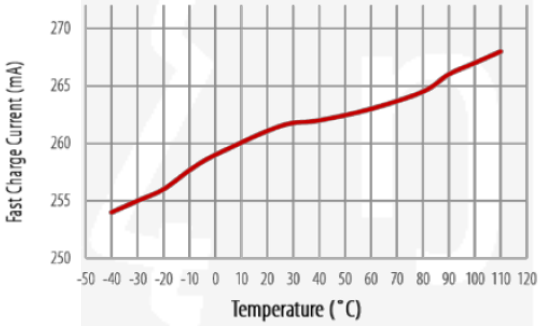
Minimum Input Regulation Voltage vs. Temperature



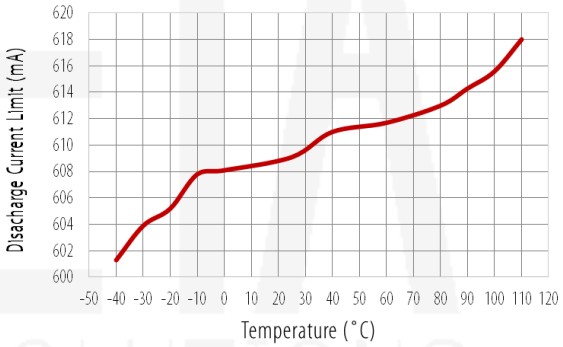
Input Current Limit Regulation vs. Temperature



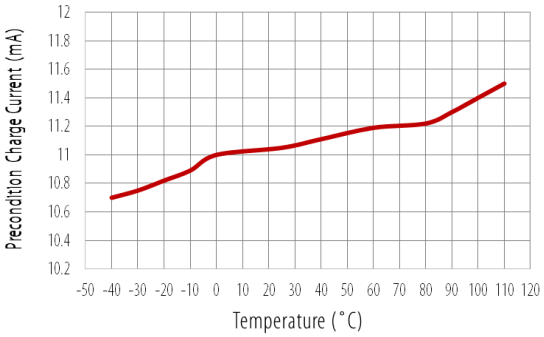
Fast Charge Current vs. Temperature



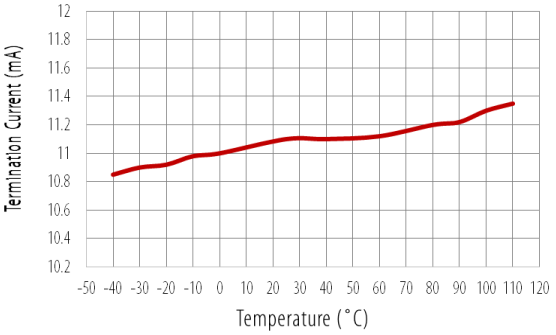
Discharge Current Limit vs. Temperature



Precondition Charge Current vs. Temperature



Termination Current vs. Temperature

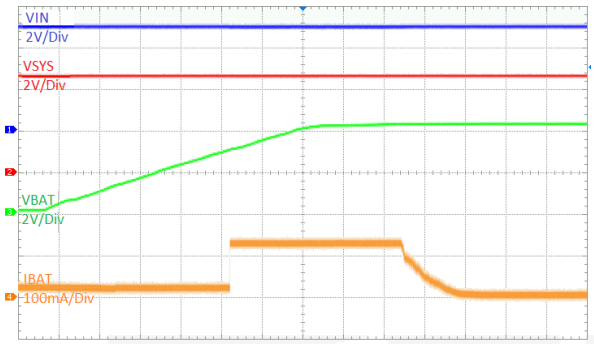


TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

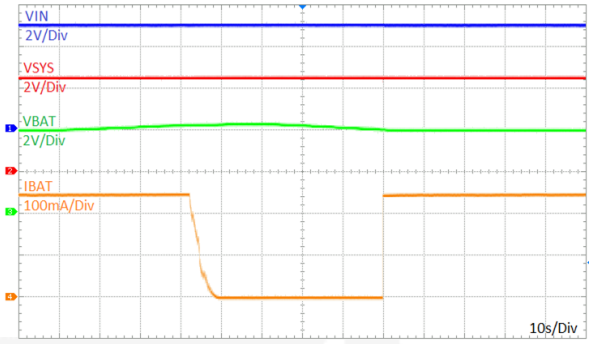
Charging Profile Curve

CH1 = V_{IN},CH2 = V_{SYS},CH3 = V_{BAT},CH4 = I_{BAT}



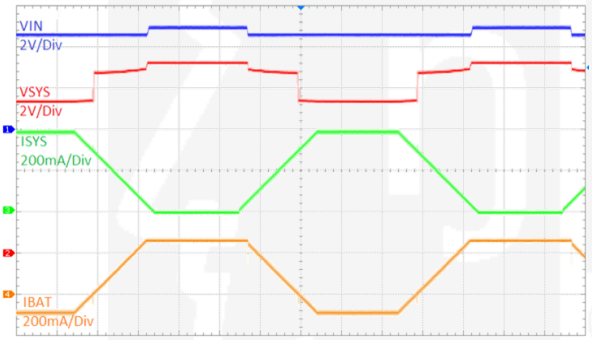
Recharging Profile Curve

CH1 = V_{IN},CH2 = V_{SYS},CH3 = V_{BAT},CH4 = I_{BAT}



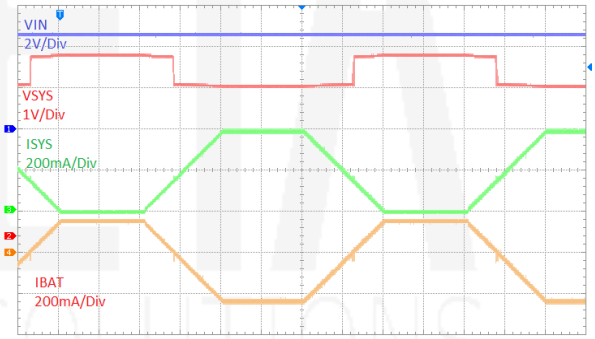
Minimum Input voltage regulation based PPM

CH1 = V_{IN},CH2 = V_{SYS},CH3 = I_{SYS},CH4 = I_{BAT}



Minimum Input voltage regulation based PPM

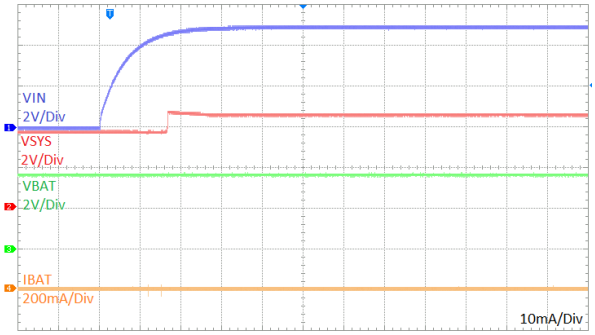
CH1 = V_{IN},CH2 = V_{SYS},CH3 = I_{SYS},CH4 = I_{BAT}



VIN Plug-in, Charge Start-Up Waveform

CH1 = V_{IN}, CH2 = V_{SYS},

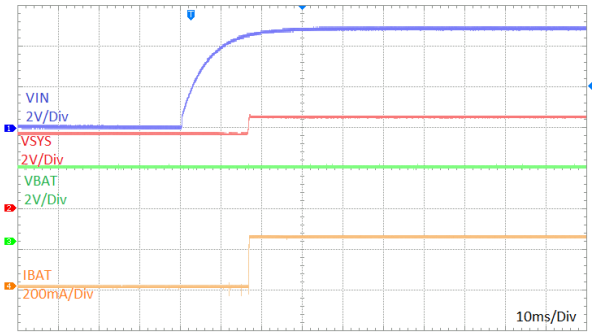
CH3 = V_{BAT},CH4 = I_{BAT}, nCE[ ] = 1



VIN Plug-in, Charge Start-Up Waveform

CH1 = V_{IN}, CH2 = V_{SYS},

CH3 = V_{BAT},CH4 = I_{BAT}, nCE[ ] = 0



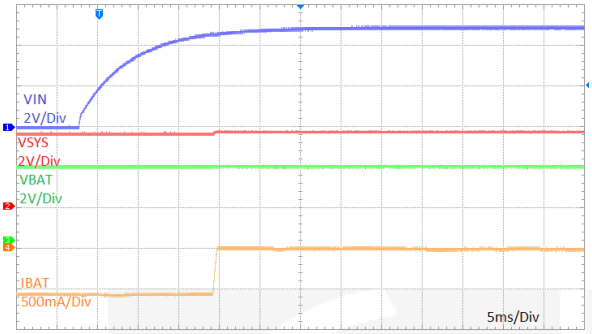
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

VIN Plug-in, Charge Start-Up to Supplement Waveform

CH1 = V_{IN}, CH2 = V_{SYS},

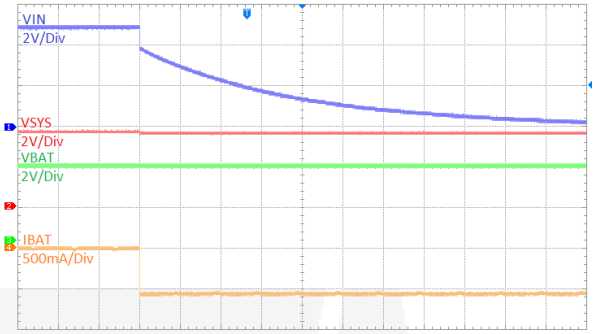
CH3 = V_{BAT},CH4 = I_{BAT}, nCE[ ] = 0



VIN Un-Plug, Charge Stop from Supplement Waveform

CH1 = V_{IN}, CH2 = V_{SYS},

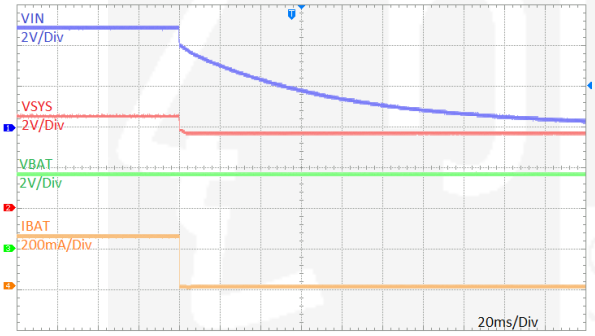
CH3 = V_{BAT},CH4 = I_{BAT}, nCE[ ] = 0



VIN Un-Plug, Charge Stop Waveform

CH1 = V_{IN}, CH2 = V_{SYS},

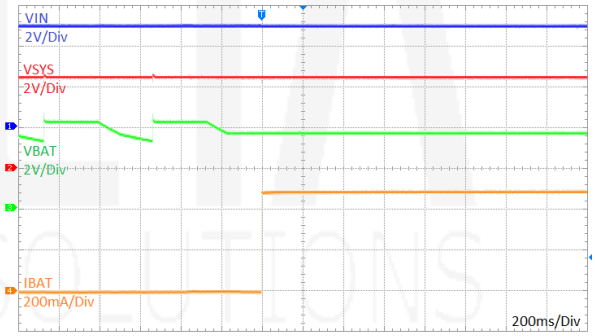
CH3 = V_{BAT},CH4 = I_{BAT}, nCE[ ] = 0



Battery Insertion

CH1 = V_{IN}, CH2 = V_{SYS},

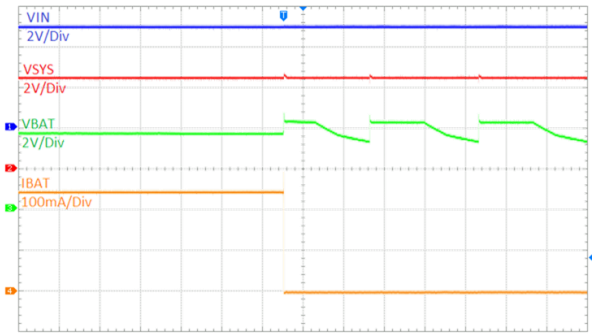
CH3 = V_{BAT},CH4 = I_{BAT}, nCE[ ] = 0



Battery Removal

CH1 = V_{VIN}, CH2 = V_{SYS},

CH3 = V_{BAT},CH4 = I_{BAT}, nCE[ ] = 0



TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

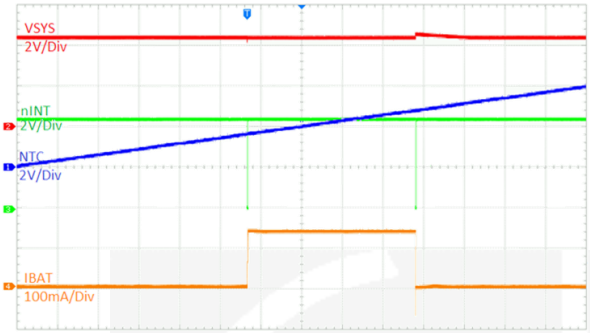
(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

NTC Voltage Rising in Charge Mode

CH1 = V_{SYS}, CH2 = V_{NTC},

CH3 = V_{nINT}, CH4 = I_{BAT},

nCE[ ] = 0, EN_NTC[ ] = 1, ENB_PCB_OTP[ ] = 1

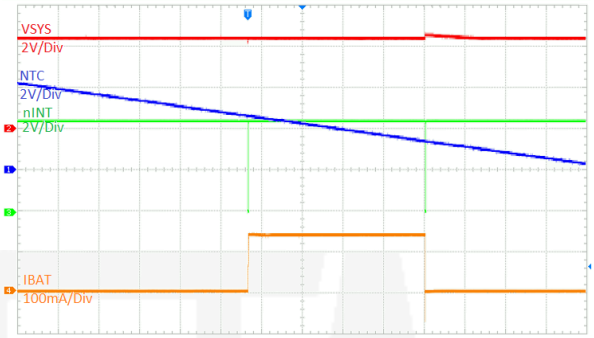


NTC Voltage Falling in Charge Mode

CH1 = V_{SYS}, CH2 = V_{NTC},

CH3 = V_{nINT}, CH4 = I_{BAT},

nCE[ ] = 0, EN_NTC[ ] = 1, ENB_PCB_OTP[ ] = 1

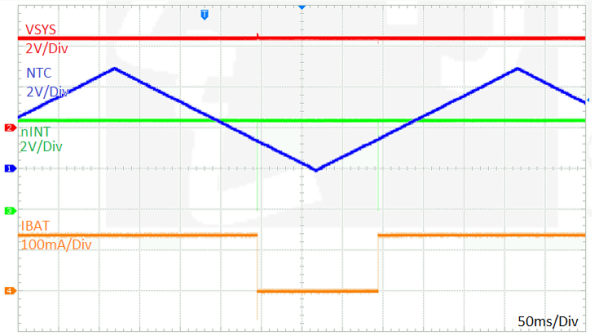


PCB_OTP in Charge Mode

CH1 = V_{SYS}, CH2 = V_{NTC},

CH3 = V_{nINT}, CH4 = I_{BAT},

EN_NTC[ ] = 1, ENB_PCB_OTP[ ] = 0

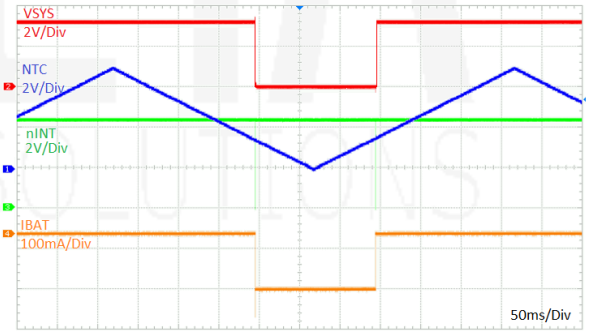


PCB_OTP in Discharge Mode

CH1 = V_{SYS}, CH2 = V_{NTC},

CH3 = V_{nINT}, CH4 = I_{BAT},

nCE[ ] = 0, EN_NTC[ ] = 1, ENB_PCB_OTP[ ] = 0



OPERATION

General Description

The ETA4662 is a single cell battery charger with power path management function for Li-Ion and Li-Polymer battery. It features pre-charging, fast charging (CC) and constant voltage (CV) charging, end-of charging termination, and auto-recharge, and built-in safe-timer preventing from being over-charged or host running out of control.

A bypass FET between VIN and SYS pin, and a battery switch FET between SYS and BAT pin is integrated for providing to complete power path management. System load is prior in getting power from the input or is switched to battery power when the input is weak or removed. Power to the battery is regulated by the battery switch FET during charging, while the input voltage, input current, voltage to system load, chip temperature and sensed external temperature are kept in priority.

错误!未找到引用源。 ***1:*** shows the power path and key circuit blocks in the ETA4662, where the Q_{BYPASS} regulates voltage to the system load and to the circuit for charging, the Q_{RVS} prevents reverse leakage from the SYS node to VIN node and the Q_{SWITCH} regulates for charging or gates the discharging from the BAT node to SYS node. The charging circuit and the discharging circuit have their own UVLO and bias, and the common circuit is powered by the higher voltage of the IN node or SYS node. The I/F is ready whenever any power is available.

The power fed to the SYS pin is recycled when watchdog times out, the host does not response to IN power input(when watchdog is forced on) or BFET_RESET[1] is set 1, to clear the running environment before system program upgrade or release from locked situations.

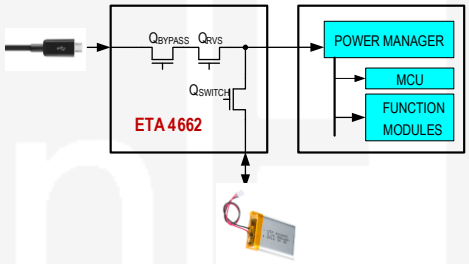


Figure 1: Power Path Management Structure

Input Detection

The device monitors the input at the VIN node. When the input is within the normal range certified by the UVLO circuit and OVP circuit for more than t_{INI} the charge circuit starts. The circuit stops or turns into OVP cut off instantly when the input voltage is lower than VIN_UVLO or is higher than VIN_OVLO, that the Q_{BYPASS} and Q_{RVS} are turned open.

错误!未找到引用源。 **2**: shows the timings relative to the input detection. The input state is certified after t_{INI} and stays for over t_{PWD}, the device outputs a pulse through the nINT. The nINT is internally pulled up to an unregulated reference voltage unless the battery is set into disconnected state. The nINT asserts pulse whenever an effective input change is certified, while the changes occurring within t_{PWM} do not assert pulse.

The watchdog timer register is set 01 once the valid input is detected and when a nINT pulse is asserted, which resumes its original setting when any writing to this device occurs. If the host does not reset the watchdog, power to the host is recycled when watchdog runs time out.

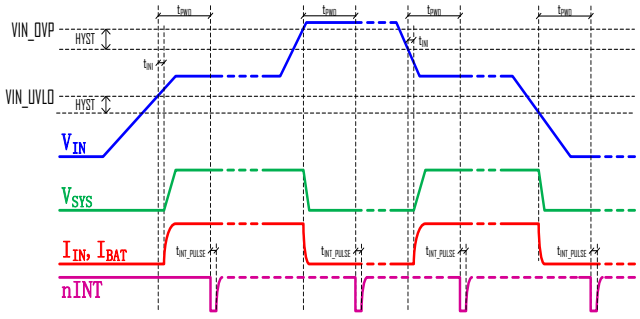


Figure 2: Input Power Detection and Operation Timings

Power Path Management

When the input is available (V_{IN} > V_{IN_UVLO}, V_{IN} - V_{SYS} > V_{HDRM}), the device intends to power the system load with input by regulating the input voltage to V_{SYS_REG} (V_{SYS} is decided by the input voltage, input current limit and battery voltage in reality). V_{SYS_REG} is programmed through REG07[3:0], The Q_{BYPASS} and Q_{SWITCH} are also manipulated by corresponding register bits, as showed in the 错误!未找到引用源。.

Table 1. FET Control by I²C

FETs	EN_HIZ = 1	CEB = 1
Q_{BYPASS}	OFF	X
Q_{SWITCH} (Charging)	X	OFF
Q_{SWITCH} (Discharging)	X	X

NOTE: X = Don't Care.

Battery Charge Profile

The charging profile managed by the device is as shown in 错误!未找到引用源。***e3***, which is segmented as following phases:

Pre-charge: If the battery voltage is less than the pre-charging threshold V_{BAT_PRE}, it charges the battery with pre-charging current, which shares the same value of the termination current programmed ITERM[3:0].

Constant-Current Charge: When battery voltage is higher than V_{BAT_PRE}, and is less than V_{BAT_REG}, it is charged with constant current that is programmed ICC[5:0] and a bit to choose scale of the current, the CC_FINE in REG0A.

Constant-Voltage Charge: When the battery voltage rises close to the battery voltage VBAT_REG[5:0], the charge current begins to decreases until the termination situation is identified.

When the charging termination function EN_TERM set via REG05 D[4] = 1, the charge cycle is considered as completed when following termination condition is identified: 1. The charge current I_{CHG} reaches the termination current threshold I_{TERM}, for over t_{TERM_DGL}; 2. Charging safe timer runs out of time if this function is enabled set via the REG05[3].

The charge status is updated to charge done once the termination condition is identified. The charge current will be terminated when termination conditions are met if TERM_TMR is not set via REG05[0]; otherwise the charge current keeps tapering off when it is set by REG05[0]=1.

During the whole charging process, the actual charge current may be less than the register setting due to other loop regulations like dynamic power management (DPM) regulation (input voltage, input current), or thermal regulation.

A new charge cycle starts when any one of the following conditions are valid:

- The input power is recycled
- Battery charging is enabled by I²C
- Auto-recharge kicks in.

Under the following conditions:

- No thermistor fault at NTC.
- No safety timer fault.
- No battery over voltage event.
- The Q_{SWITCH} is not forced to turn off

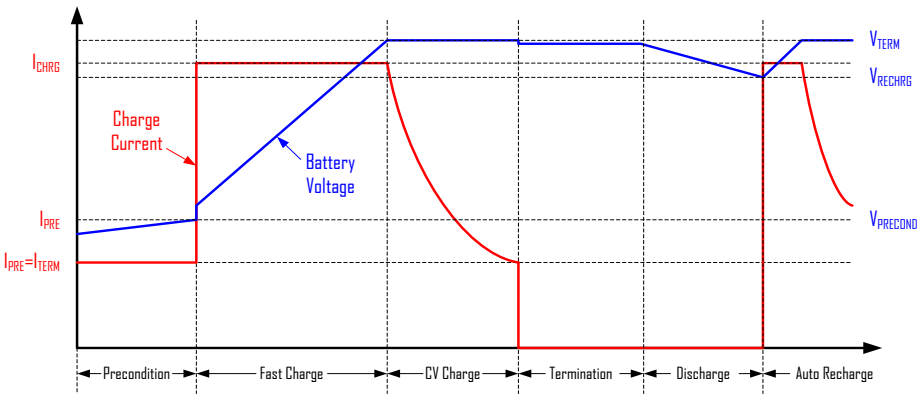


Figure 3: Battery Charge Profile

Battery Over-Voltage Protection

This device is designed with a built-in battery over-voltage limit about VBAT_OVP higher than the VBAT_REG. When the battery over-voltage event occurs, the device immediately suspends the charging and asserts a fault. A discharging path is turned on when the battery OVP keeps.

Input Current and Input Voltage Based Power Path Management

To meet the input source (USB usually) maximum current limit specification, the IC features the input current based power management by continuously monitoring the input current. The total input current limit can be programmed via the I2C to prevent the input source from over-loaded.

If the preset input current limit is higher than the rating of the input source, the back-up input voltage based power management also works to prevent the input source from being over-loaded. Either the input current limit or the input voltage limit is reached, the Q_{BYPASS} between IN and SYS pin will be regulated so that the total input power will be limited. As a result the system voltage drops, once the system declines to minimum value of the VSYS_REG - DVSYS_LOW and VIN - DVIN_LOW, the charge current will be reduced to prevent the system voltage from dropping further.

The voltage based dynamic power management (DPM) will regulate the input voltage to VIN_MIN when the load is over the input power capacity.

The VIN_MIN set via I^2C should be at least 250mV higher than VBAT_REG to make sure the stable operation of the regulator.

Battery Supplement Mode

As mentioned above, the charge current is reduced to keep the input current or input voltage in regulation when DPM happens. If the charge current is reduced to zero and the input source is still overloaded due to heavy system load, the system voltage starts to decrease. Once the system voltage falls $V_{SYS-BAT\_LOW}$ below the battery voltage, the device enters battery supplement mode and the ideal diode mode will be enabled. The Q_{SWITCH} is regulated to maintain the V_{BAT}-V_{SYS} at $V_{SYS-BAT\_REG}$ when I_{DSCHG} (supplement current) × R_{ON_BAT} is lower than $V_{SYS-BAT\_REG}$, in the case the I_{DSCHG} x R_{ON_BAT} is higher than $V_{SYS-BAT\_REG}$, the Q_{SWITCH} is fully turned on to keep ideal forward voltage. During system load decreasing, once V_{SYS} is higher than V_{BAT} + $V_{SYS-BAT\_HIGH}$, the ideal diode mode will be disabled. 错误!未找到引用源。 shows the dynamic power management and battery supplement mode operation profile.

When VIN is not available, the device operates in discharge mode, the Q_{SWITCH} is always fully on to reduce the loss.

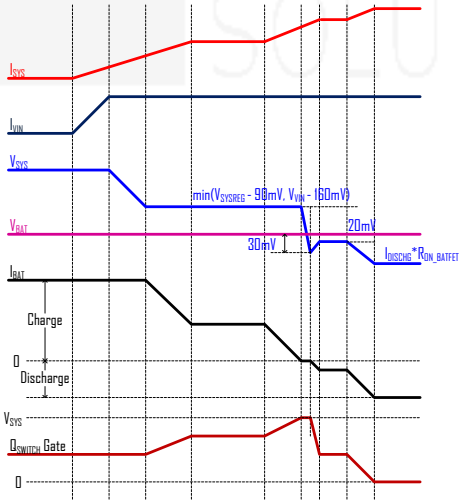


Figure 4: Dynamic Power Management and Battery Supplement Operation Profile

Battery Regulation Voltage

The battery voltage for the constant voltage regulation phase is V_{BAT_REG}. When battery is float, the BAT pin voltage varies between V_{BAT_REG} - V_{RECH} and V_{BAT_REG}.

Thermal Regulation and Shutdown

The device continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches preset limit of T_{J_REG}, the device starts to reduce the charge current to prevent higher power dissipation. The programmable thermal regulation thresholds help system design to meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via TJ_REG[1:0].
When the junction temperature reaches T_{J_SHDN} that is slightly higher than most high programmable thermal regulation temperature threshold, both the Q_{BYPASS} and Q_{SWITCH} are turned off.

NTC Sensing and VDD Gating

The NTC pin allows the device to sense the battery temperature using the thermistor usually available in the battery pack to ensure a safe operating environment of the chip. A resistor with appropriate value should be connected from VDD pin to NTC pin and the thermistor is connected from NTC pin to ground. The voltage on NTC pin is determined by the resistor divider whose divide ratio depends on temperature. The device internally sets a pre-determined upper and lower bound of the divide ratio for NTC cold and NTC hot.
In ETA4662, I²C default setting is the PCB OTP; user can change the function through I²C:

Table 2. NTC Function Selection

I²C CONTROL		FUNCTION
EN_NTC	EN_PCB OTP	
0	x	Disable
1	1	NTC
1	0	PCB OTP

The VDD powering from battery when not powered by the supply applied on the IN pin is gated via setting a register bit DIS_VDD.
When PCB OTP is selected, if the NTC pin voltage is lower than the NTC hot threshold, both the Q_{BYPASS} and Q_{SWITCH} are off. The PCB OTP fault also will set the NTC_FAULT status to 1 to show the fault. The operation will resume once the NTC pin voltage is higher than the NTC hot threshold.
NTC function only works in charge mode. Once NTC pin voltage falls out of this divide ratio which means the temperature is outside the safe operating range, the device will stop the charging and report it on status bits. Charging will automatically resume after the temperature falls back into the safe range.

Safety Timer

The device provides both the pre-charge and charge safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 1hr when battery voltage is lower than V_{BAT_PRE}. The charge safety timer starts when the battery enters constant-current or constant-voltage charge. The user can program charge safety timer through I²C. The safety timer feature can be disabled via I²C.
The following actions restart the safety timer:

- A new charge cycle is kicked in.
- Write REG01[3] from 1 to 0 (charge enable)
- Write REG05[3] from 0 to 1 (safety timer enable)
- Write REG02[7] from 0 to 1 (software reset)
- Write REG0A[4] from 0 to 1 (software power recycle)

Host Mode and Default Mode

Upon power on reset, the device starts in the watchdog timer expiration state, or default mode. All the registers are in the default settings, when the EN_HIZ = 0, CEB = 1, power input and battery discharge are enabled.
Watchdog timer works in both charge and discharge mode. When the watchdog timer runs time out, the power to load system recycles by cutting off the Q_{SWITCH} and Q_{BYPASS} for the default of t_{RST_DUR} and all the registers in this device reset to the default value.

And to save the quiescent current during discharge mode, the watchdog timer can be turned off during discharge mode by set the EN_WD_DISCHG bit to 0.
Any write to the device transits it to host mode. If the watchdog timer (WATCHDOG[1:0]) is not disabled, the host has to reset the watchdog timer regularly by writing 1 to REG02 WD_RST bit before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the device goes back into default mode. The watchdog timer limit can also be programmed or disabled by host control.
When the WATCHDOG[1:0] is set to 00, then the watchdog timer is disabled under both charge mode and discharge mode no matter EN_WD_DISCHG status is.
The operation could also be turned to default mode when one of the following conditions are valid:

- Refresh input without battery
- Re-insert battery with no VIN
- Register reset REG_RST bit is set 1

Battery Discharge Function

If battery is connected and the input source is missing, the Q_{SWITCH} is fully on when VBAT is above the VBAT_UVLO threshold. The low Ron Q_{SWITCH} minimizes the conduction loss during discharge. The quiescent current of the device is as low as 6μA in this mode. By setting REG0A[3] = 1, the Q_{SWITCH} keeps on with sensing circuit off, to further reduce the quiescent current to below 1μA. The low on-resistance and low quiescent current help extend the running time.

Over-Discharge Current Protection

The over-discharge current protection is effective in discharge mode and supplement mode. Once the IBAT exceeds discharge current limit programmed through the REG03[7:4], the Q_{SWITCH} cuts off after t_{DSCHG_CUT} and the device resumes conducting after t_{RETRY}. Besides, if the discharge current goes high to hit IDSCHG_S, the Q_{SWITCH} cuts off instantly.
When the battery voltage falls below VBAT_UVLO programmed through the REG01[2:0], the Q_{SWITCH} cuts off to prevent over discharge.
When REG0A[3] is set 1, the Q_{SWITCH} is forced on and the over-discharge is not sensed during battery discharge. The REG0A[3] is reset 0 when effective power input to the IN applied. If the REG0A[3] is set when only the power input applied, attaching to detaching the battery does not make any change to the status.

System Short Circuit Protection

When system short circuit occurs, the Q_{SWITCH} cuts the BAT to SYS path and the Q_{BYPASS} limits the current input through the IN to SYS path. If the system short circuit remains, the die temperature goes high to cause thermal shut down.
The ETA4662 features V_{SYS} node short circuit protection for both V_{IN} to V_{SYS} path and BAT to VSYS path.

- ***V_{IN} to V_{SYS} path:*** The ETA4662 starts activate hard short protection after V_{SYS} goes greater than 1.5V once. This means the IC allows to start-up with full current limit. Once this condition occurs, if V_{SYS} falls below 1.5V, and I_{IN} is found over the protection threshold, Q_{SWITCH}, Q_{BYPASS} and Q_{RVS} are turned off immediately. And the operation of the IC goes into the hiccup mode. Beside hard short protection, at any time V_{SYS} is lower than 1.5V, while the setting input current limit is reached, I_{IN} is regulated at I_{IN_LIM} the hiccup mode also starts after a 60μs delay. The interval of the hiccup mode is 800us.
- ***BATT to SYS path:*** Once I_{BAT} is found over the 3.7A protection threshold, both the LDO FET and the BATT FET are turned off immediately and the operation of the IC goes into the hiccup mode. Besides, while the battery discharge current limit threshold is reached, the hiccup mode also starts after a 60μs delay. The interval of the hiccup mode is 800us.
- Particularly, if the system short circuit happens when both input and battery are present, the protection mechanism of both paths will work, the faster one dominates the hiccup operation.

Interrupt to Host (INT)

This device also has an alert mechanism which can output an interrupt signal via nINT pin to notify the system on the operation by outputting low for t_{INT_PULSE}. Any of the events listed below triggers the nINT output.

- Good input source detected
- UVLO or input over voltage detected
- Charge completed
- Charging status change

- Any fault recorded in REG09 (input fault, thermal fault, safety timer fault, battery OVP fault, NTC fault) and in REG08[7] occurs.

When any fault occurs, this device sends out nINT pulse and latches the fault state in register bits correspondingly. After the device quit the fault state, the fault bit could be released to 0 after the host reads. The NTC fault is not latched and always reports the current thermistor conditions.

The INT signal can be masked when the corresponding control bit is set, which means, even the event which causes the INT signal happened, user can just keep the nINT high when the INT signal is not acceptable in the application, via setting the INT control bit in REG06[4:0].

The nINT is pulled up to an unregulated low voltage that is not high enough to most logic circuit (in the circuit the device loads), to avoid unexpected creeping powering and leakage during power recycling and in shipping mode; the nINT is pulled up to a high voltage in other states. Both the low voltage and high voltage are internally generated and pull up is weak and could be over-driven externally.

Battery Disconnection Function

In the application that the battery is not removable, it's essential to disconnect the battery from the system for shipping mode in stock or to allow the recycle of the system power during the application. ETA4662 provides both shipping mode (shown in Table 3) and system power recycling for different applications.

Table 3. Shipping Mode Control

ITEMS	ENTER SHIPPING MODE	EXIT SHIPPING MODE	
	FET_DIS = 1	nINT Pin H to L for 2s	VIN Plug In
LDO FET	X (To disable LDO FET (VIN to VSYS), set EN_HIZ[ ]=1)	X	ON
Q_{SWITCH} (Charging)	OFF	ON	ON (2s Later)
Q_{SWITCH} (Discharging)	OFF	ON	ON (2s Later)

NOTE: x = Don't Care.

The FET_DIS bitfor battery disconnection control. If this bit is set to 1, it enters shipping mode after a delay time, which can be programmed by EN_SHIP_DGL[1:0], the Q_{SWITCH} turns off and the FET_DIS bit refresh to 0 after the Q_{SWITCH} is off. Pulling down nINT pin or VIN is detected, the device wakes up from shipping mode.

This device can also reuse nINT pin or watchdog overflow signal to cut off the path from battery to system under the condition need to recycle the system power. Once the logic at nINT pin set to low for more than t_{INT_OFF} which can be programmed via t_{RST_DGL} or watchdog time is overflow, the battery is disconnected from the system by turning off the Q_{SWITCH} and Q_{BYPASS}, the off state lasts for t_{INT_ON} which can be programmed via t_{RST_DUR}, then the Q_{SWITCH} and Q_{BYPASS} will be automatically turned on and system is powered again. During the off period, the nINT pin is biased to a lower voltage.

The waveforms of power recycling are shown in 错误!未找到引用源。5.

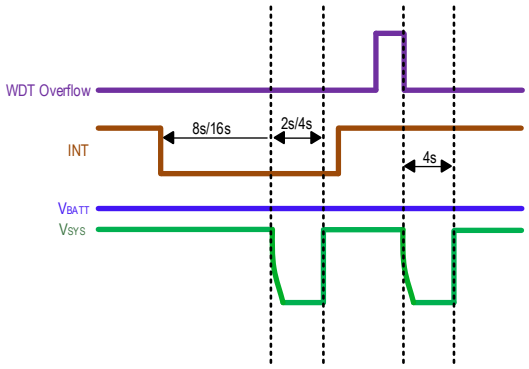


Figure 5. Power Recycling Waveforms

OPERATION DIAGRAM

Main State Machine

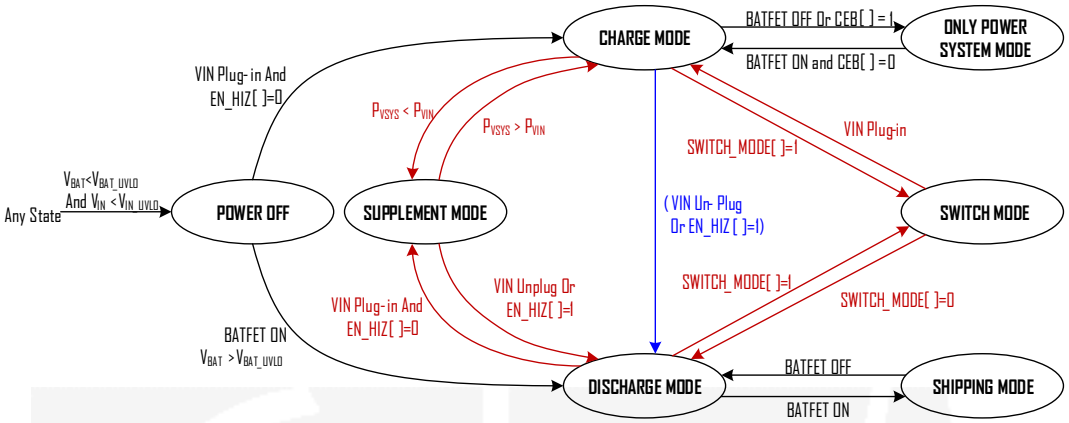


Figure 6: State Machine Conversion

HOST Control Flow Chart

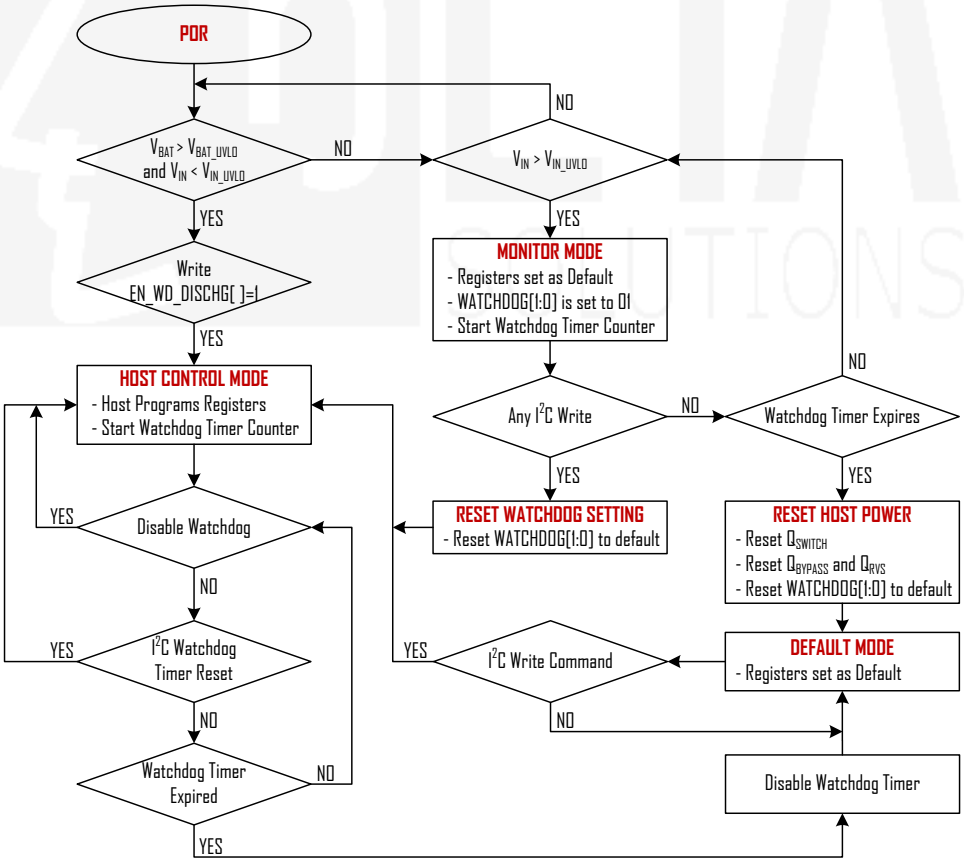


Figure 7: Default Mode and Host Mode Selection

Charger Flow Chart

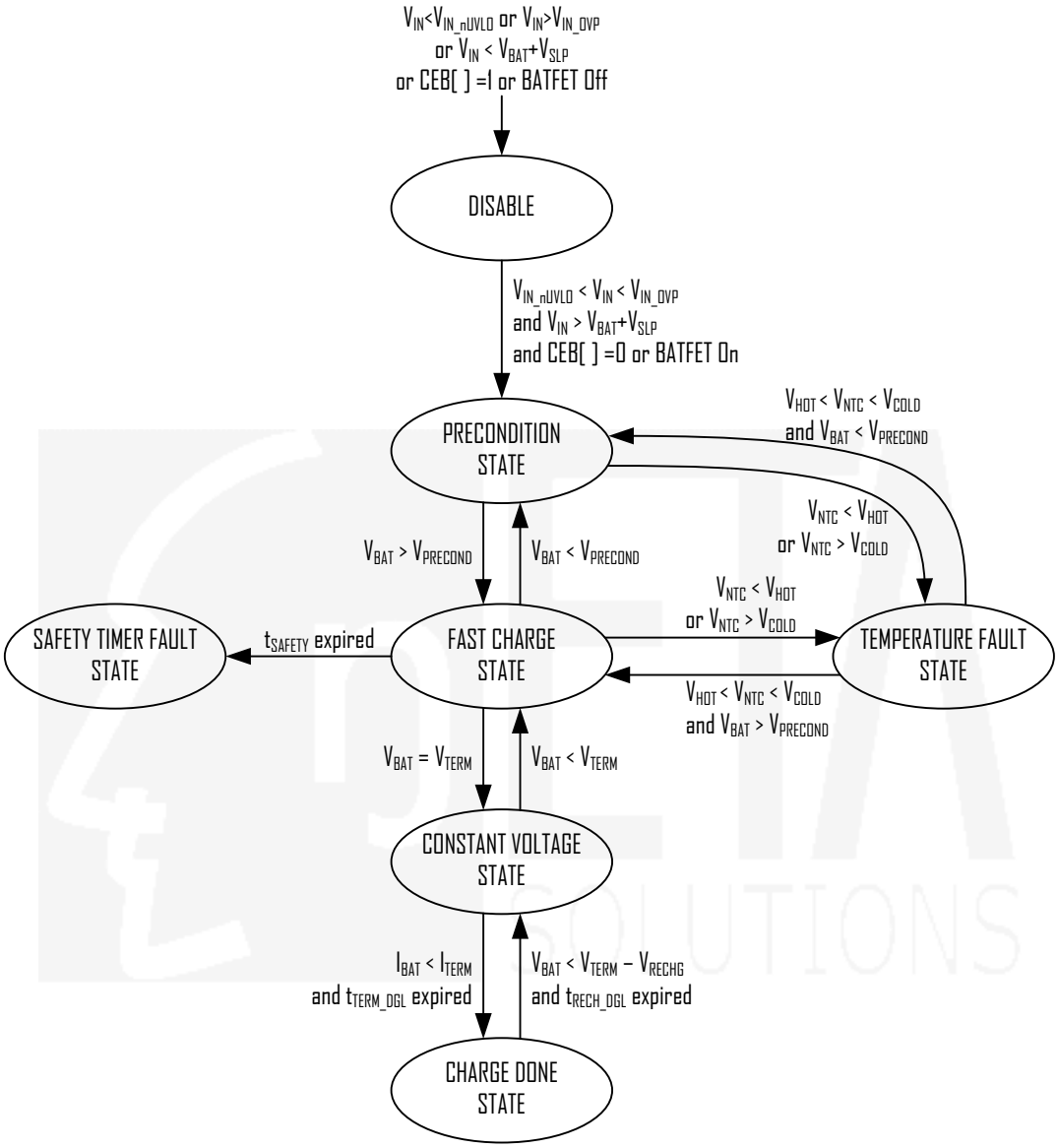


Figure 8: Charger Flow Chart

System Short Circuit Protection

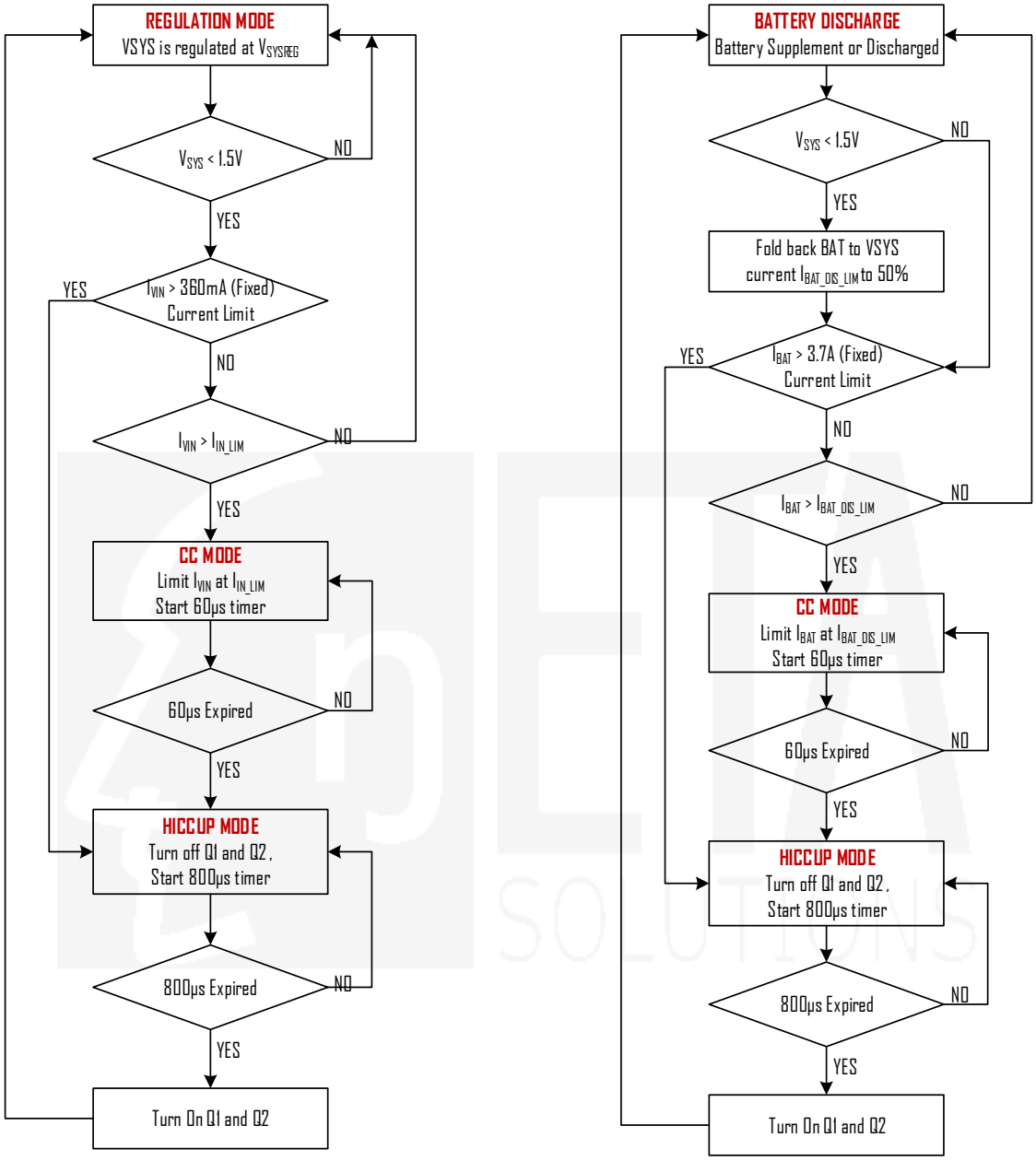


Figure 9: System Short Circuit Protection

APPLICATION INFORMATION

Resistor Choose for NTC Sensor for Battery Temperature Monitor

NTC pin uses a resistor divider from input source (VDD) to sense the battery temperature. The two resistors RT1 and RT2 allow the high temperature limit and low temperature limit to be programmed independently, as shown in Figure. In other word, this device can fit most type of NTC resistor and different temperature operation range requirement with the two extra resistors.

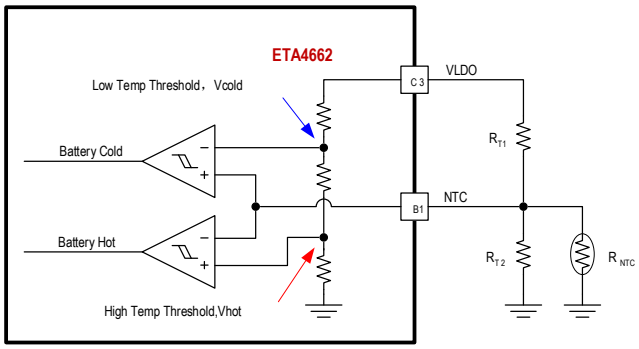


Figure 10: NTC Function Block

For a given NTC thermistor, RT1 and RT2 values depend on the type of the NTC resistor and can be calculated with following equations:

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD} \times V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD} \times V_{HOT}) \times R_{NTCH}}$$

$$R_{T1} = \frac{1 - V_{COLD}}{V_{COLD}} \times \frac{R_{T2} \times R_{NTCL}}{R_{T2} + R_{NTCL}}$$

Where R_{NTCH} is the value of the NTC resistor at high temperature of the required temperature operation range, and R_{NTCL} is the value of the NTC resistor at low temperature.

Resistor Choose for NTC Sensor for HOT PCB Temperature Monitor

ETA4662 features PCB temperature monitor function. When this function is set, Function will operate in both Charge and Discharge Mode and COLD detect is invalid. Same equations with Battery Temperature Monitor will be used normally.

External Capacitor Selection

Like most low-dropout regulators, the ETA4662 requires external capacitors for regulator stability and voltage spike immunity. The device is specifically designed for portable applications requiring minimum board space and smallest components, these capacitors must be correctly selected for good performance.

Input Capacitor

An input capacitor is required for stability, at least, a 1μF capacitor has to be connected between IN to GND for stable operation over full load current range. Basically, it is OK to have more output capacitance than input, as long as the input is at least 1μF.

Output Capacitor

This device is designed specifically to work with a very small ceramic output capacitor. A ceramic capacitor (dielectric types X5R or X7R) >2.2μF is suitable in the ETA4662 application circuit. For this device, the output capacitor should be connected between VSYS pin and GND pin with thick trace and small loop area.

BAT to GND Capacitor

The capacitor from the BAT pin to GND pin is also necessary for ETA4662. A ceramic capacitor (dielectric types X5R or X7R) >2.2μF is suitable for the ETA4662 application circuit.

VDD to GND Capacitor

The capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

PCB Layout Guideline

Put external capacitors as close to this device as possible to make sure the smallest input inductance and the ground impedance. The PCB trace to connect the capacitor between VDD and GND is very important, and it should be put very close to this device.

The GND for the I²C wire should be clean, and it should not be very close to the GND. I²C wire should be put in parallel.

EVALUATION KIT DESIGN

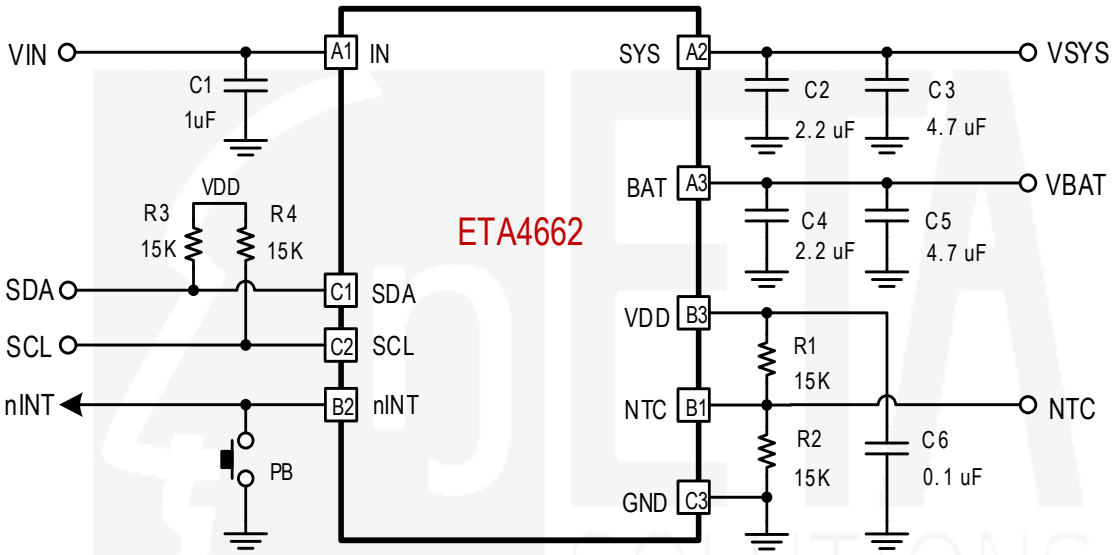


Figure 11: ETA4662 EVKIT Design

Table 4: ETA4662 EVKIT BOM List

QTY	DEVICE	VALUE	DESCRIPTION	PACKAGE	RECOMMENDED MANUFATURE
1	C1	1μF	20V Ceramic Capacitor (X5R or X7R)	0603	TBD
2	C2, C4	2.2μF	10V Ceramic Capacitor (X5R or X7R)	0603	TBD
2	C3, C5	4.7μF	10V Ceramic Capacitor (X5R or X7R)	0603	TBD
1	C6	100nF	10V Ceramic Capacitor (X5R or X7R)	0603	TBD
4	R1, R2, R3, R4	15kΩ	Resistor	0603	TBD
1	PB		Push Button		TBD

I²C REGISTER MAP

I²C Address is set 0ExH as default and can be programmable after power up by change ADDR[2:0] bits.

Table 5: Register General Description

REGISTER NAME	ADDRESS	RD/WR	DESCRIPTION	DEFAULT
REG00	00xH	RD/WR	Input Source Control Register	1001 1111
REG01	01xH	RD/WR	Power on configuration register	1010 1100
REG02	02xH	RD/WR	Charge Current Control Register	0000 1111
REG03	03xH	RD/WR	Dis-charge/ Termination Current	1001 0001
REG04	04xH	RD/WR	Charge Voltage Control Register	1010 0011
REG05	05xH	RD/WR	Charge Termination/Timer Control Register	0111 1010
REG06	06xH	RD/WR	Miscellaneous Operation Control Register	1100 0000
REG07	07xH	RD/WR	System Voltage Regulation Register	0011 0111
REG08	08xH	RD	System Status Register	0000 0000
REG09	09xH	RD	Fault Register	0000 0000
REG0A	0AxH	RD/WR	I²C Address and Miscellaneous Configuration Register	1110 0000
REG0B	0BxH	RD	Device ID Register	0000 0000

Table 6: Input Source Control Register - Memory Location: 00xH. Reset State: 1001 1111

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	V_{INDPM}[3:0]	1	REG_RST	RD/WR	640mV	Range: 3.88V – 5.08V Default:4.6V(1001) Offset:3.88V
6		0	REG_RST	RD/WR	320mV	
5		0	REG_RST	RD/WR	160mV	
4		1	REG_RST	RD/WR	80mV	
3	I_{IN_LIM}[3:0]	1	REG_RST	RD/WR	240mA	Range: 50mA – 500mA Default:500mA(1111) Offset:50mA
2		1	REG_RST	RD/WR	120mA	
1		1	REG_RST	RD/WR	60mA	
0		1	REG_RST	RD/WR	30mA	

Table 7: Power On Configuration Register - Memory Location: 01xH. Reset State: 1010 1100

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	T_{RST_DGL}[1:0]	1	REG_RST WD_RST	RD/WR	00: 8s 01: 12s 10: 16s (Default) 11: 20s	Pull INT low time period to disconnect the battery.
6		0	REG_RST WD_RST	RD/WR		
5	T_{RST_DUR}	1	REG_RST WD_RST	RD/WR	0: 2s 1: 4s (Default)	The Q_{BYPASS} and Q_{SWITCH} Lasts Off Time Before Auto-On
4	EN_HIZ	0	REG_RST WD_RST	RD/WR	0: Enabled 1: Disabled	Default: Enable(0)
3	CEB	1	REG_RST WD_RST	RD/WR	0: Charge Enable 1: Charge Disabled	Default: Charge Disable(1)

2	V_{BAT_UVLO}[2:0]	1	REG_RST WD_RST	RD/WR	360mV	Battery UVLO Threshold: Range: 2.4V – 3.03V Default:2.76V(100) Offset:2.4V
1		0	REG_RST WD_RST	RD/WR	180mV	
0		0	REG_RST WD_RST	RD/WR	90mV	

Table 8: Charge Current Control Register - Memory Location: 02xH. Reset State: 0000 1111

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	REG_RESET	0	REG_RST	RD/WR	0: Keep current setting 1: Reset	Once write REG_RST[ ] = 1, longer than 10ms needed before write REG_RST[ ] = 0. In the time between these 2 actions, can write or read anything else
6	WD_RESET	0	REG_RST WD_RST	RD/WR	0: Normal 1: Reset	Default: Normal(0)
5	I_{CHG}	0	REG_RST WD_RST	RD/WR	256mA	Fast Charge Current setting: Range:8mA-456mA(111000) Default:128mA(001111) Offset:8mA
4		0	REG_RST WD_RST	RD/WR	128mA	
3		1	REG_RST WD_RST	RD/WR	64mA	
2		1	REG_RST WD_RST	RD/WR	32mA	
1		1	REG_RST WD_RST	RD/WR	16mA	
0		1	REG_RST WD_RST	RD/WR	8mA	

Table 9: Dis-charge/ Termination Current Register - Memory Location: 03xH. Reset State: 1001 0001

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	I_{DSCHG}[3:0]	1	REG_RST WD_RST	RD/WR	1600mA	BAT to SYS Discharge Current Limit Configuration: Range: 400mA – 3.2A Default:2A(1001) Offset:200mA
6		0	REG_RST WD_RST	RD/WR	800mA	
5		0	REG_RST WD_RST	RD/WR	400mA	
4		1	REG_RST WD_RST	RD/WR	200mA	
3	I_{TERM}[3:0]	0	REG_RST WD_RST	RD/WR	16mA	Termination and Precondition Current configuration: Range:1mA – 31mA Default: 3mA(0001)
2		0	REG_RST WD_RST	RD/WR	8mA	

1		0	REG_RST WD_RST	RD/WR	4mA	Offset:1mA
0		1	REG_RST WD_RST	RD/WR	2mA	

Table 10: Charge Voltage Control Register - Memory Location: 04xH. Reset State: 1010 0011

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	V_{BAT_REG}[5:0]	1	REG_RST WD_RST	RD/WR	480mV	Battery Termination Voltage Configuration Range:3.6V – 4.545V Default: 4.2V(101000) Offset:3.6V
6		0	REG_RST WD_RST	RD/WR	240mV	
5		1	REG_RST WD_RST	RD/WR	120mV	
4		0	REG_RST WD_RST	RD/WR	60mV	
3		0	REG_RST WD_RST	RD/WR	30mV	
2		0	REG_RST WD_RST	RD/WR	15mV	
1	V_{BAT_PRE}	1	REG_RST WD_RST	RD/WR	0: 2.8V 1: 3V(Default)	Pre-charge to Fast Charge Threshold: Rising Threshold
0	V_{RECH}	1	REG_RST WD_RST	RD/WR	0: 100mV 1: 200mV (Default)	Battery Recharge Threshold: Delta voltage below V_{BAT_REG}

Table 11: Charge Termination/Timer Control Register - Memory Location: 05xH. Reset State: 0111 1010

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	EN_WD_DISCHG	0	REG_RST	RD/WR	0:Disable(Default) 1: Enable	Watchdog Control in Discharge Mode
6	WATCHDOG[1:0]	1	REG_RST	RD/WR	00:Disable 01:40s	Default: 160s(11)
5		1	REG_RST	RD/WR	10:80s 11:160s	
4	EN_TERM	1	REG_RST WD_RST	RD/WR	0:Disable 1:Enable(Default)	Charge Termination Enable
3	EN_TIMER	1	REG_RST WD_RST	RD/WR	0:Disable 1:Enable(Default)	Safety Timer Configuration
2	CHG_TMR [1:0]	0	REG_RST	RD/WR	00:3hrs 01:5hrs	Default Fast Charge Timer: 5hrs(01)
1		1	WD_RST	RD/WR	10:8hrs 11:12hrs	
0	TERM_TMR	0	REG_RST WD_RST	RD/WR	0:Disable (Default) 1:Enable	Termination Timer Control

Table 12: Miscellaneous Operation Control Register - Memory Location: 06xH. Reset State: 1100 0000

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	EN_NTC	1	REG_RST WD_RST	RD/WR	0: Disable 1: Enable (Default)	Battery Thermal Monitor Enable
6	TMR2X_EN	1	REG_RST WD_RST	RD/WR	0: Normal safety timer 1: 2X extended safety timer (Default)	Enable long Charger Timer Fault in DPM
5	BFET_DIS	0	REG_RST	RD/WR	0: Enable(Default) 1: Disable	Battery FET Q_{SWITCH} Disable
4	PG_INT_CTL	0	REG_RST WD_RST	RD/WR	0: No Mask (Default) 1: Mask	Mask Power Good to nINT Indication
3	EOC_INT_CTL	0	REG_RST WD_RST	RD/WR	0: No Mask (Default) 1: Mask	Charge Complete to nINT Indication
2	CHG_STAT_INT_CTL	0	REG_RST WD_RST	RD/WR	0: No Mask (Default) 1: Mask	Charge Status Change to nINT Indication
1	NTC_INT_CTL	0	REG_RST WD_RST	RD/WR	0: No Mask (Default) 1: Mask	NTC Fault to nINT Indication
0	BATTOVP_INT_CTL	0	REG_RST WD_RST	RD/WR	0: No Mask (Default) 1: Mask	Battery OVP to nINT Indication

Table 13: System Voltage Regulation Register - Memory Location: 07xH. Reset State: 0011 0111

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	ENB_PCB_OTP	0	REG_RST WD_RST	RD/WR	0: Enable (Default) 1: Disable	PCB Over-Temperature Protection Function
6	DIS_VINDPM	0	REG_RST WD_RST	RD/WR	0: Enable (Default) 1: Disable	Enable VIN DPM Loop
5	TJ_REG[1:0]	1	REG_RST WD_RST	RD/WR	00: 60ºC 01: 80 ºC 10: 100 º C 11: 120ºC (Default)	Thermal Regulation Threshold Configuration
4		1	REG_RST WD_RST	RD/WR		
3	V_{SYS_REG}[3:0]	0	REG_RST	RD/WR	400mV	System Voltage Regulation Configuration: Range:4.2V – 4.95V Default:4.55V Offset:4.2V
2		1	REG_RST	RD/WR	200mV	
1		1	REG_RST	RD/WR	100mV	
0		1	REG_RST	RD/WR	50mV	

Table 14: System Status Register - Memory Location: 08xH. Reset State: 0000 0000

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	WTD_FAULT	0	N/A	RD	0: Normal 1: Watchdog Timer Expiration	I²C Watchdog Timer Fault Status
6	NO_IN_ILIM	0	N/A	RD	0: Use IN_ILIM 1: Disable IN_ILIM	VIN Current Limit
5	ILIM_ADD200mA	0	N/A	RD	0: Normal IN_ILIM 1: Add 200mA	

4	CHG_STAT[1:0]	0	N/A	RD	00: Not Charging 01: Pre Charge 10: Charge 11: Charge Done	Charge Status
3		0	N/A	RD		
2	PPM_STAT	0	N/A	RD	0: Not in PPM 1: In PPM	Power Management Status
1	PG_STAT	0	N/A	RD	0: Power Fail 1: Power Good	Power Good Status
0	THERM_STAT	0	N/A	RD	0: No Thermal Regulation 1: In Thermal Regulation	Thermal Regulation Status

Table 15: Fault Register - Memory Location: 09xH. Reset State: 0000 0000

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	EN_SHIP_DGL[1:0]	0	REG_RST	RD/WR	00: 1s (Default) 01: 2s 10: 4s 11: 8s	Enter Shipping Mode Deglitch Time Configuration
6		0	REG_RST	RD/WR		
5	VIN_FAULT	0	N/A	RD	0: Normal 1: Input fault (OVP or bad source)	VIN Condition Status
4	THEM_SD	0	N/A	RD	0: Normal 1: Thermal Shutdown	Thermal Shutdown Status
3	BAT_FAULT	0	N/A	RD	0: Normal 1: Battery OVP	Battery Status
2	STMR_FAULT	0	N/A	RD	0: Normal 1: Safety Timer Expiration	Safety Timer Status
1	NTC_HOT	0	N/A	RD	0: Normal 1: HOT Condition	NTC Pin in HOT Condition: Always be '0' when PCB_OTP Function is set.
0	NTC_COLD	0	N/A	RD	0: Normal 1: COLD Condition	NTC Pin in COLD Condition: Always be '0' when PCB_OTP Function is set.

Table 16: Address OTP Register - Memory Location: 0AxH. Reset State: 1110 0000

BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	ADDR[2:0]	1	N/A	RD	000: 00H 001: 02H 010: 04H 011: 06H 100: 08H 101: 0AH 110: 0CH 111: 0EH(Default)	I²C Address Configuration
6		1		RD		
5		1		RD		
4	COLD_RESET	0	N/A	RD/WR	BATFET Reset: 0: Not Reset BATFET 1: Reset BATFET	Auto cleared after BATFET Reset
3	SWITCH_MODE	0	REG_RST	RD/WR	0: Normal Power Path 1: For BATFET On without Current Limit	Force SWITCH Mode:
2	DIS_VDD	0	REG_RST	RD/WR	0:Enable to Battery Power 1:Disable Battery Power	VDD Output Voltage Pin Setting:

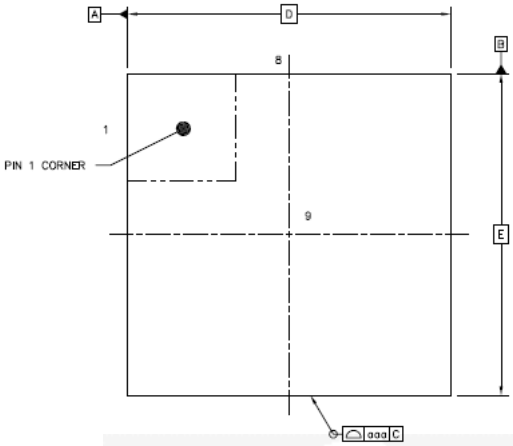
1	DIS_VINOVP	0	REG_RST	RD/WR	0:Enable 1:Disable	VIN Over Voltage Lock Out Disable
0	CC_FINE	0	N/A	RD/WR	0: Keep default ICHRG as ICHRG[5:0] defined 1: Program ICHRG with all specs of ICHRG[5:0] divided by 4.	Finer turn charge current

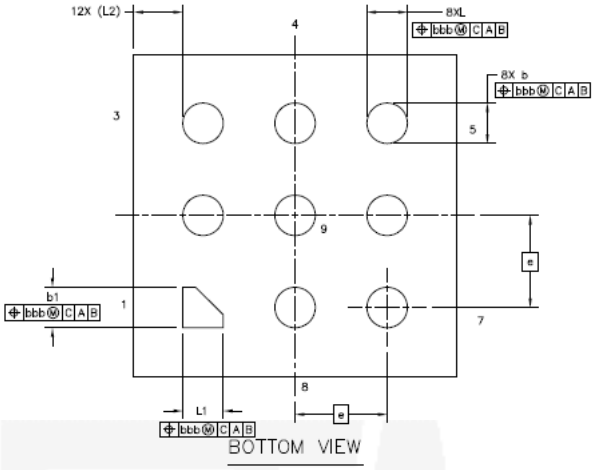
Table 17: ETA Solution Part Identify - Memory Location: 0BxH. Reset State: 00000000

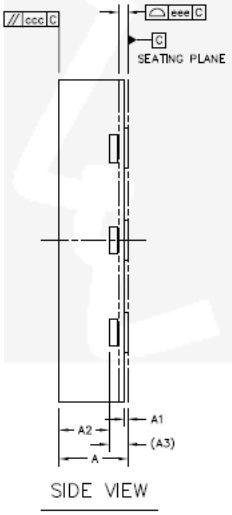
BIT	NAME	POR	RESET BY	RD/WR	FUNCTION	NOTE
7	ETA_CODE[7:0]	0	N/A	RD	0000 0000: ETA4662 All Other: Wrong IC	Identification Code
6		0	N/A	RD		
5		0	N/A	RD		
4		0	N/A	RD		
3		0	N/A	RD		
2		0	N/A	RD		
1		0	N/A	RD		
0		0	N/A	RD		

PACKAGE OUTLINE DIMENSIONS

FCQFN-9L 1.75x1.75mm

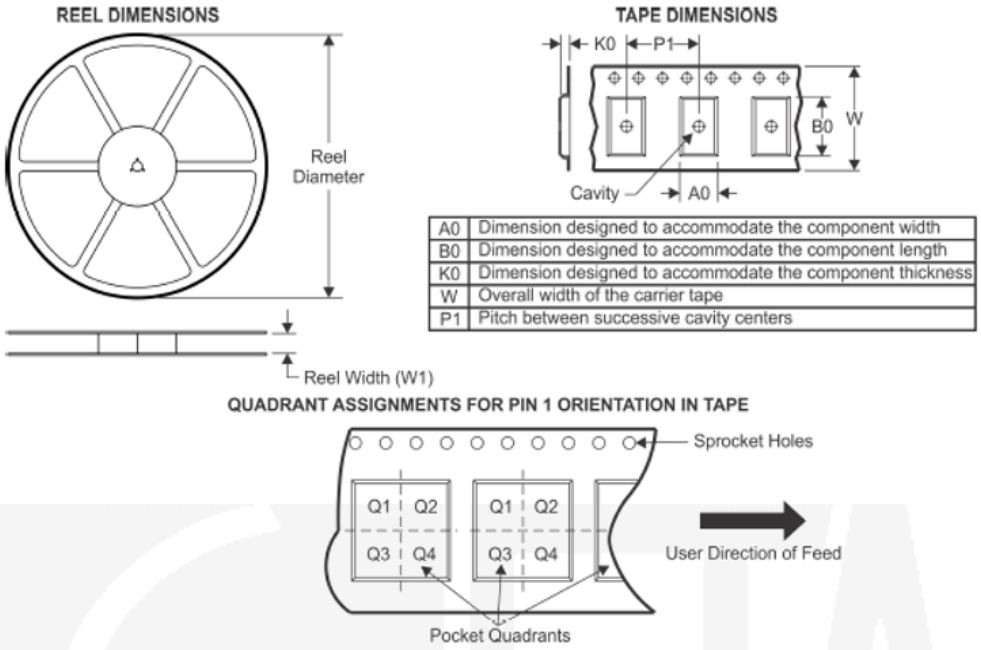






		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.32	0.37	0.4
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.27	---
L/F THICKNESS		A3		0.102 REF	
LEAD WIDTH		b	0.17	0.22	0.27
		b1	0.12	0.22	0.32
BODY SIZE	X	D		1.75 BSC	
	Y	E		1.75 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.17	0.22	0.27
		L1	0.12	0.22	0.32
LEAD EDGE TO PACKAGE EDGE		L2		0.265 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA4662FQFJ	QFN1.75*1.75-9	9	3000	178	9.5	2.00	2.00	0.50	4	8	Q1