Programmable Single Cell Li-Ion Battery Charger with Power Path Management

DESCRIPTION

The ETA4098 is a flexibly programmable highly-integrated single cell Li-Ion and Li-polymer battery charger with power path management. It features pre-charging, fast charging(CC) and constant voltage(CV) charging, end-of charging termination, and auto-recharge. The built-in safe-timer monitors input voltage, input current, chip temperature, external temperature and load current, preventing from being damaged due to excessive high current and over-discharging. The charge current and charge termination current are programmable by flexible external resistors.

The power path management function features a low dropout regulator from the input to the system and a low Rdson switch from the battery to the system, ensuring the continuous power supply to the system.

ETA4098 is available in a FCQFN-9L package.

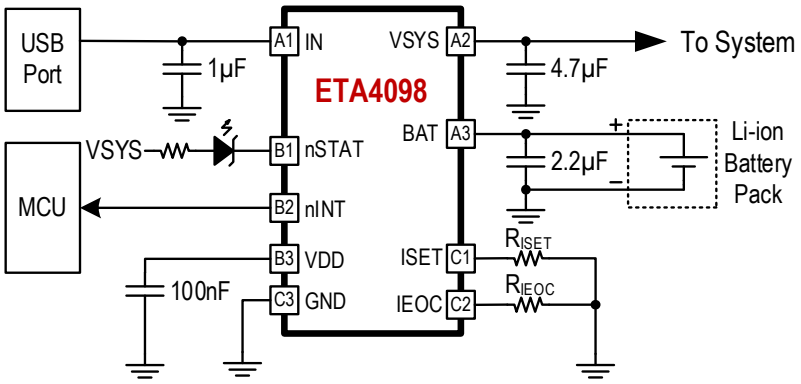
FEATURES

- Fully Autonomous Charger for Single Cell Li-Ion and Li-Polymer Battery
- 4.2/4.35V Charge Termination Voltage
- 21V Maximum Input Voltage Rating with Over-Voltage Protection
- ±0.5% Charging Voltage Accuracy
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection
- System Reset Function
- Built-In Battery Disconnection Function
- Thermal Limiting Regulation on Chip
- FCQFN-9L 1.75mmx1.75mm

APPLICATIONS

- Wearable Devices
- IoT Gadgets

TYPICAL APPLICATION

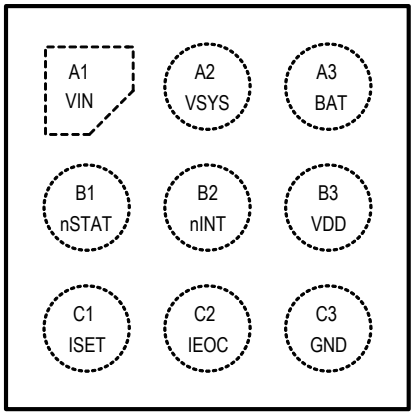


ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA4098FQFJ	FCQFN1.75x1.75-9	STYW	3000
ETA4098V435FQFJ	FCQFN1.75x1.75-9	S4YW	3000

PIN CONFIGURATION

Top View



FCQFN1.75x1.75-9L

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN Pin Voltage to GND ..... -0.3V to 28V
VIN to GND Discharge Current 5mA
VSYS to GND Voltage..... -0.3V to 5.5V
BAT Pins Voltage to GND ..... -1V to 6V
All Other Pins Voltage to GND ..... -0.3V to 6V
VSYS, BAT to ground current..... Internally limited
Operating Temperature Range.....–40°C to 85°C
Storage Temperature Range.....–55°C to 150°C

Thermal Resistance	θ_{JC}	θ_{JA}	
FCQFN-9	12	114	°C/W

Lead Temperature (Soldering, 10 seconds) ..260°C
ESD HBM (Human Body Mode)..... 2KV
ESD MM (Machine Mode).....200V

ELECTRICAL CHARACTERISTICS

(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER		TESTCONDITIONS	MIN	TYP	MAX	UNIT
VIN INPUT AND BATTERY CONDITION						
V_{IN_UVLO}	VIN Input Under Voltage Lock Out Threshold	V_{IN} Falling	3.63	3.73	3.83	V
$V_{IN\_UVLO\_HYS}$	VIN_UVLO Hysteresis	V_{IN} Rising		170		mV
V_{IN_OVP}	VIN Input Over Voltage Protection Threshold	V_{IN} Rising	18.5	19	19.5	V
$V_{IN\_OVP\_HYS}$	VIN_OVP Hysteresis	V_{IN} Falling		500		mV
V_{IN_CLAMP}	VIN Input Clamp Voltage	Test for having 1mA clamp current.	20			V
I_{VIN_SHUNT}	VIN Input Discharge Current	V_{IN} = 21V		5		mA
V_{HDRM}	Sleep-Mode Entry Threshold, VIN - VBAT	V_{IN} Falling vs. V_{BAT}		85		mV
V_{HDRM_EXIT}	Sleep-Mode Exit Hysteresis	V_{IN} Rising vs. V_{BAT}	100	130	160	mV
V_{BAT}	BAT Input Voltage Range				5	V
t_{INI}	Input Detection Deglitch Time	For either under-voltage or over-voltage		250		µs

PARAMETER		TESTCONDITIONS	MIN	TYP	MAX	UNIT
t_{PWD}	Input Power Detection Time	Time before reporting power on or off	50	75	100	ms
t_{INT_PULSE}	nINT Output Pulse Duration			250		μs
V_{BAT_UVLO}	Battery Under Voltage Lockout Threshold	V_{BAT} Falling	2.3	2.4	2.5	V
$V_{BAT\_UVLO\_HYS}$	VBAT_UVLO Hysteresis	V_{BAT} Falling, V_{BAT_UVLO}=2.76V		210		mV
V_{BAT_OVP}	Battery Over Voltage Protection Threshold	V_{BAT} Rising, higher than V_{TERM}		130		mV
$V_{BAT\_OVP\_HYS}$	VBAT_OVP Hysteresis	V_{BAT} Falling		70		mV
$I_{BAT\_DSCHGOVP}$	Battery Over-Voltage Discharge			5		μA
SUPPLY CURRENT CONDITION						
I_{Q_VIN}	Input Quiescent Current	V_{IN}=5.5V, I_{CHG}=0A, I_{SYS}= 0A		250		μA
I_{Q_VBAT}	Battery Quiescent Current	V_{IN}=5V, I_{SYS}=0A, Charge done, V_{BAT}=4.3V		5		μA
		V_{IN}=GND, V_{BAT}=4.35V, I_{VSYS}= 0A		12		
POWER PATH MANAGEMENT						
V_{SYS_REG}	Regulated System Output Voltage Accuracy	V_{IN} = 5.5V, R_{VSYS}=100Ω	4.50	4.55	4.60	V
V_{SYS_OVP}	System Over Voltage Protection to Discharger	V_{SYS} Rising, As Percentage of V_{SYS_REG}		10		%
$V_{SYS\_OVP\_HYS}$	V_{SYS_OVP} Hysteresis	V_{SYS} Falling, As Percentage of V_{SYS_REG}		5		%
R_{VSYS_DIS}	V_{SYS} Discharge Resistance	V_{SYS} > V_{SYS_OVP}		400		Ω
V_{INDPM}	Input Minimum Voltage Regulation		4.50	4.60	4.70	V
I_{IN_ILIM}	Input Current Limiting		440	470	500	mA
R_{ON_LDOFET}	VIN to VSYS Switch On Resistance	VIN=4.5V, IVSYS=100mA		200		mΩ

PARAMETER		TESTCONDITIONS		MIN	TYP	MAX	UNIT
R_{ON_BATFET}	BATFET On Resistance	V_{IN} < 2V, V_{BAT}=3.5V, I_{SYS}=100mA			100		mΩ
I_{BAT_LIM}	Battery Discharge Currrent Limit				2000		mA
I_{DISCHG_S}	Discharge Short Circuit Limit				3.7		A
I_{VIN_LOWSYS}	Maximum VIN Current to Shutoff	VSYS falling below V_{HSHORT}			360		mA
V_{HSHORT}	VSYS Short Detection Threshold				1.5		V
t_{CUTDEL}	Delay before Over Current Cut				60		μs
t_{RETRY}	Delay before Retry after Cut				800		μs
V_{FWD}	Ideal Diode Forward Voltage in Supplement Mode	10mA Discharge Current			20		mV
DYNAMIC POWER MANAGEMENT AND BATTERY SUPPLEMENT							
DV_{SYS_LOW}	SYS Drop for Lowering Charging				90		mV
DV_{IN_LOW}	IN Drop for Lowering Charging				160		mV
$DV_{SYS-BAT\_LOW}$	SYS-BAT Drop for Supplement				30		mV
$DV_{SYS-BAT\_REG}$	SYS-BAT Regulation in Supplement				22.5		mV
$DV_{SYS-BAT\_HIGH}$	SYS-BAT drop for Exit Supplement				20		mV
BATFET RESET							
t_{RST_DGL}	Reset by nINT				8		s
t_{RST_DUR}	BATFET Off Lasting Time				2		s
BATTERY CHARGER							
V_{TERM}	Battery Charge Termination Voltage	I_{BAT} = 1mA	ETA4098	4.179	4.2	4.221	V
			ETA4098V435	4.329	4.35	4.371	

PARAMETER		TESTCONDITIONS	MIN	TYP	MAX	UNIT
	Regulation (Aging and pre-condition drift included in 0°C~50°C)					
V_{ISET}	ISET Pin Regulation Voltage	$V_{BAT} > V_{PRECHG}$		0.8		V
		$V_{BAT} < V_{PRECHG}$		0.25		
V_{IEOC}	IEOC Pin Trip Threshold			0.25		V
I_{CHRG}	Fast Charge Current	R_{ISET} = 8kΩ	80	100	120	mA
		R_{ISET} = 3.2kΩ	220	250	280	
		R_{ISET} = 2kΩ	360	400	440	
I_{PRE}	Pre-charge Current	$I_{PRE} = I_{TERM}$		I_{TERM}		mA
I_{TERM}	Charge Termination Current Threshold	R_{IEOC} = 20kΩ		12.5		mA
		R_{IEOC} = 10kΩ		25		
		R_{IEOC} = 5kΩ		50		
$V_{PRECOND}$	Precondition to Fast Charge Threshold	Rising, $V_{PRECOND}$ = 3.0V	2.9	3.0	3.1	V
$V_{PRECOND\_HYS}$	Precondition to Fast Charge Hysteresis	Falling		90		mV
V_{RECH}	Auto Recharge Voltage Threshold	Below V_{TERM},	70	100	130	mV
t_{TERM_DGL}	Termination Deglitch Time			200		ms
t_{RECH_DGL}	Battery Auto-Recharge Deglitch Time			200		ms
t_{SAFETY}	Fast Charge Safety Timer			5		Hrs
THERMAL PROTECTION						
T_{J_REG}	Junction Temperature Regulation			120		˚C
T_{J_SHDN}	Thermal Shutdown Threshold			150		˚C
$T_{J\_SHDN\_HYST}$	Thermal Shutdown Hysteresis			20		˚C
LOGIC IO PIN SPECIFICATION, nINT, SCL, SDA						
V_{IL}	Input Low Logic Voltage Threshold	Falling			0.4	V
V_{IH}	Input High Logic Voltage	Rising	1.3			V

PARAMETER		TESTCONDITIONS	MIN	TYP	MAX	UNIT
	Threshold					
V_{OL}	Output Low Level	I_{SINK} = 5mA			0.4	V

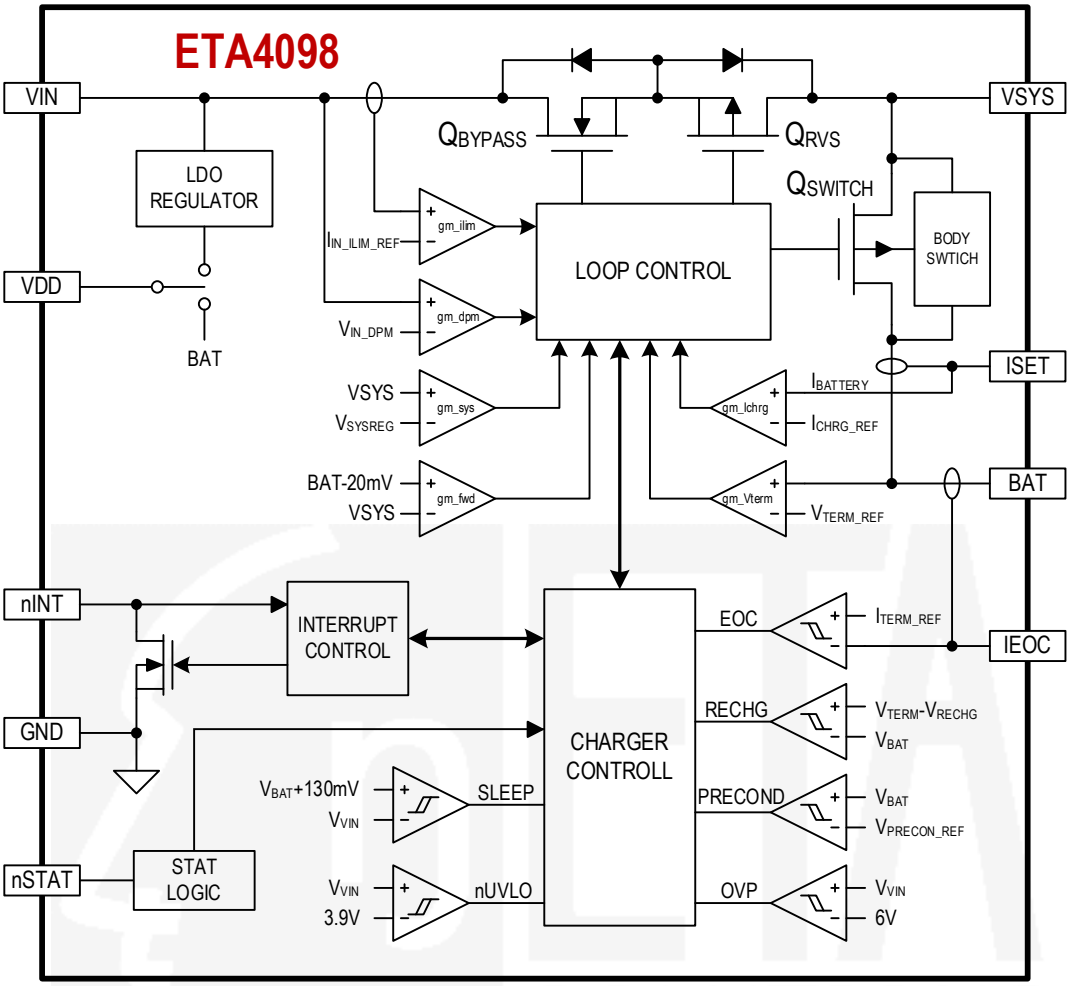
NOTE: For lowering the bias current in the chip, and also to avoid biasing external circuit with output of nINT, the logic high level of the nINT should be an buffered level of an internal reference in range of 1.8~2.5V, at a roughly regulated voltage level.

PIN DESCRIPTION

PIN#	PIN NAME	TYPE	DESCRIPTION
C2	IEOC	AIO	Termination Charge Current Configuration Input Pin. Bypass a resistor to GND to set up termination threshold.
C1	ISET	AIO	Charge Current Configuration Input Pin. Bypass a resistor to GND to set up charge current. Bring ISET pin to a voltage greater than 1.1V to suspend charging.
B1	nSTAT	AIO	Charge status pin. Pull low when charge in progress. Open drain for other conditions.
B2	nINT	AIO	Interrupt Output and Battery FET Reset Input pin. The nINT pin sends charging status and fault notification to the host. This pin is also used to reset the system from the battery. Refer to "*Interrupt to Host (nINT)*" and "*Battery Disconnection Function*" sections for detail information.
A1	VIN	P	Input Power Pin. Place a ceramic capacitor from IN pin to GND as close as possible to this device.
A2	VSYS	P	System Power Supply. Place a ceramic capacitor from SYS pin to GND as close as possible to this device.
A3	BAT	P	Battery Pin. Place a ceramic capacitor from BAT pin to GND as close as possible to IC.
B3	VDD	P	Internal Control Power Supply Pin. Connect a 0.1μF ceramic cap from this pin to GND.
C3	GND	P	Ground Pin
NA	EP	P	Thermal Pad. Connect to GND on PCB.

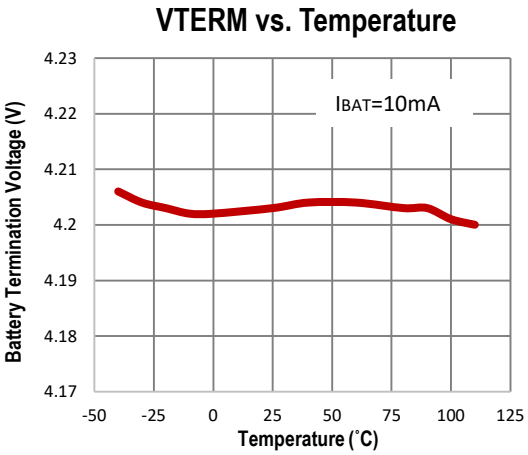
Note: AIO = Analog Input and Output; DI = Digital Input; DO = Digital Output; DIO = Digital Input and Output; P = Power.

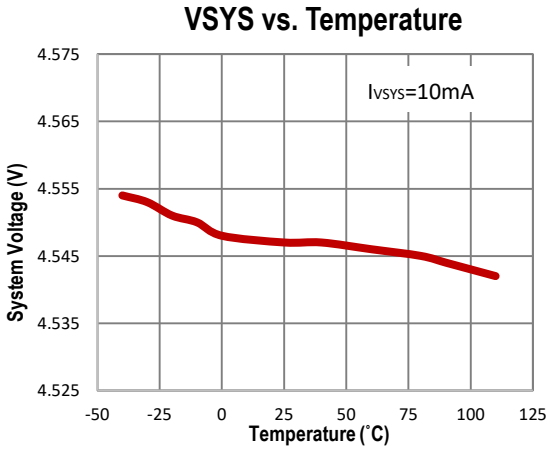
FUNCTIONAL BLOCK DIAGRAM

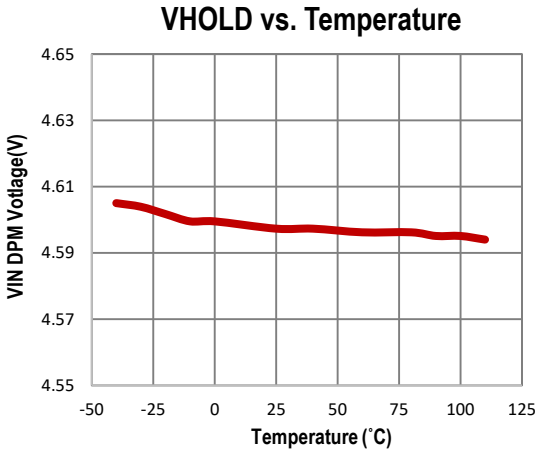


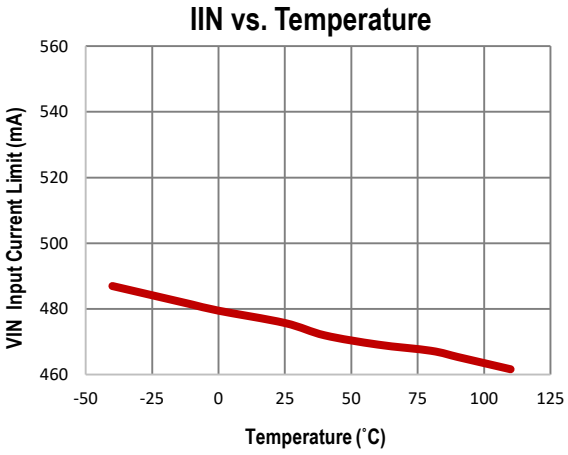
TYPICAL PERFORMANCE CHARACTERISTICS

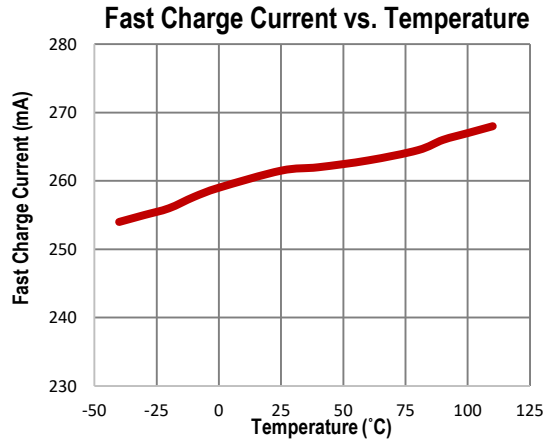
(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

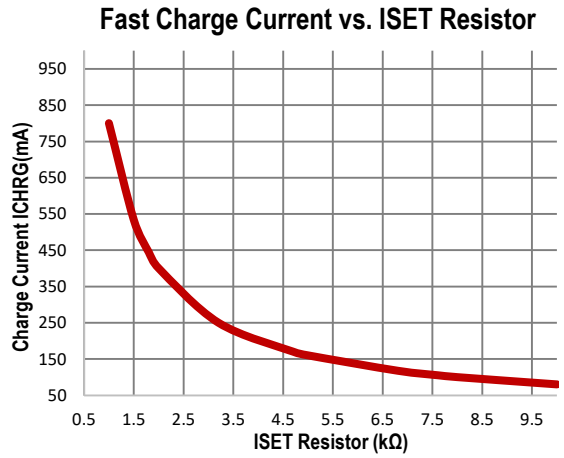








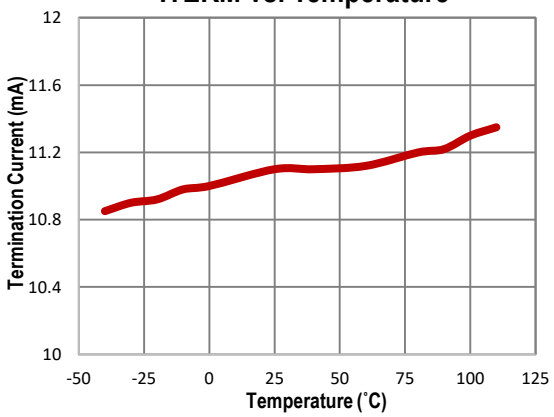




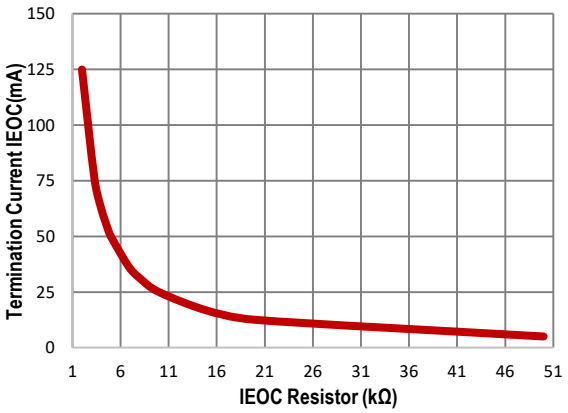
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

ITERM vs. Temperature

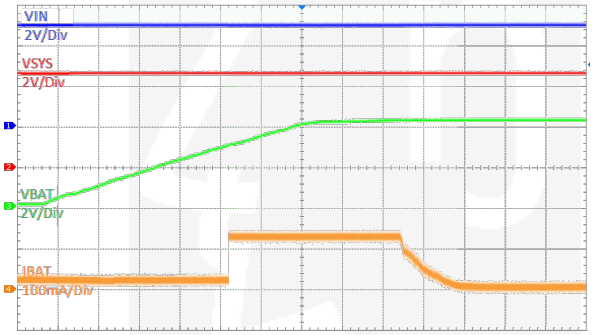


ITERM vs. IEOC Resistor



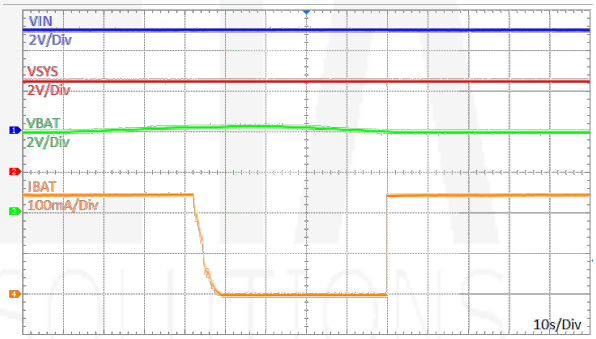
Charging Profile Curve

CH1 = VIN, CH2 = VSYS, CH3 = VBAT, CH4 = IBAT



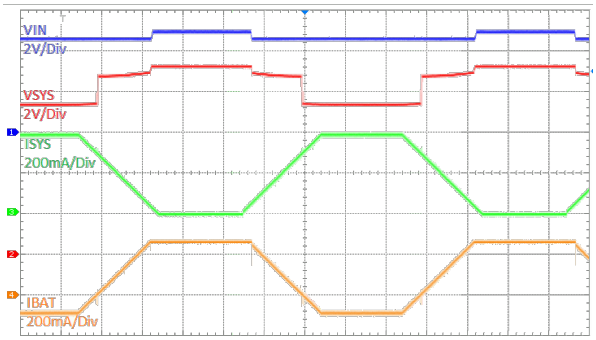
Recharging Profile Curve

CH1 = VIN, CH2 = VSYS, CH3 = VBAT, CH4 = IBAT



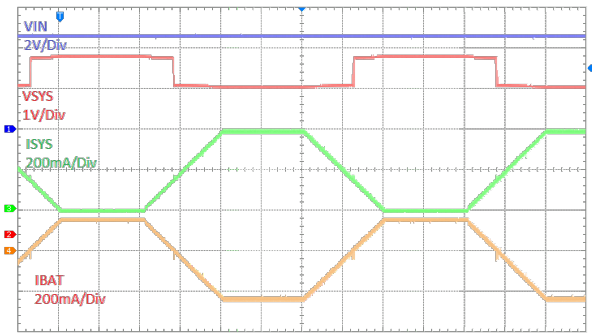
Minimum Input voltage regulation based PPM

CH1 = VIN, CH2 = VSYS, CH3 = ISYS, CH4 = IBAT



Minimum Input voltage regulation based PPM

CH1 = VIN, CH2 = VSYS, CH3 = ISYS, CH4 = IBAT

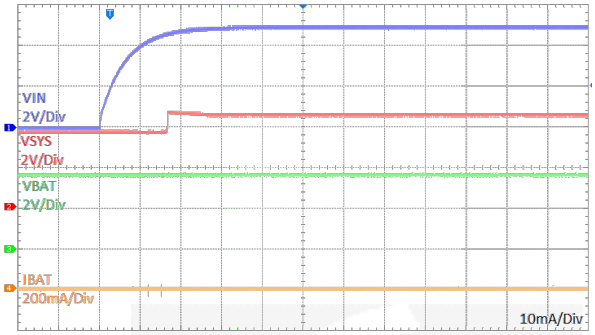


TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(V_{IN} =5V, V_{BAT}=4.2V unless otherwise specified. Typical values are at TA = 25°C.)

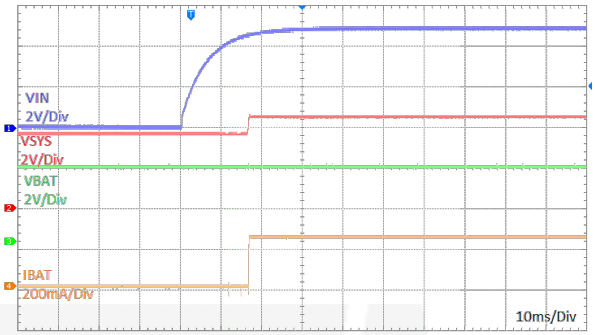
VIN Plug-in, Charge Start-Up Waveform

CH1 = VIN, CH2 = VSYS, CH3 = ISYS,
CH4 = IBAT, Force V_{ISET} > 1.2V



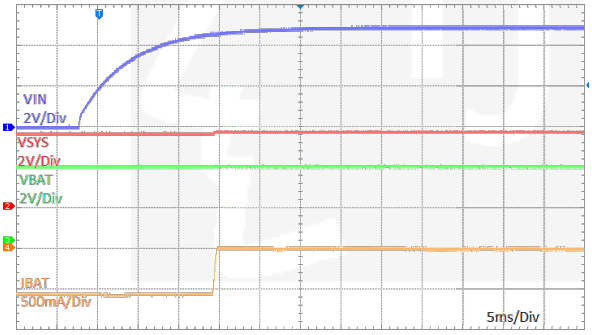
VIN Plug-in, Charge Start-Up Waveform

CH1 = VIN, CH2 = VSYS, CH3 = ISYS,
CH4 = IBAT, Not Force V_{ISET} > 1.2V



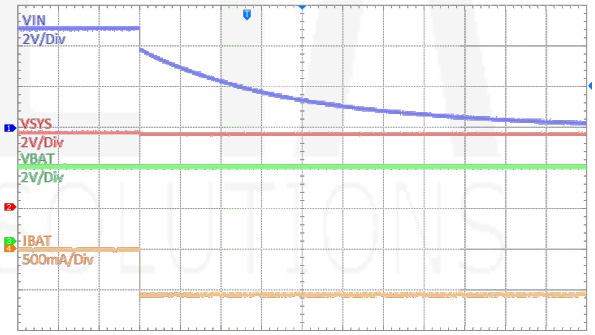
VIN Plug-in, Charge Start-Up to Supplement Waveform

CH1 = VIN, CH2 = VSYS, CH3 = ISYS,
CH4 = IBAT



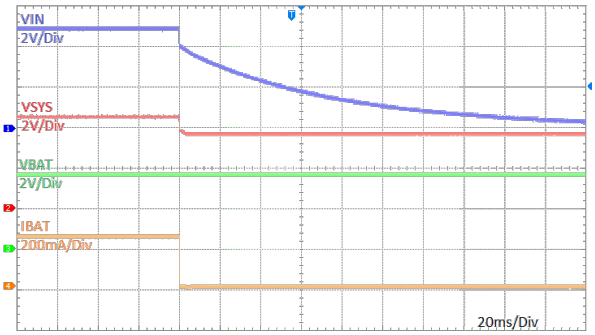
VIN Un-Plug, Charge Stop from Supplement Waveform

CH1 = VIN, CH2 =VSYS, CH3 = ISYS,
CH4 = IBAT



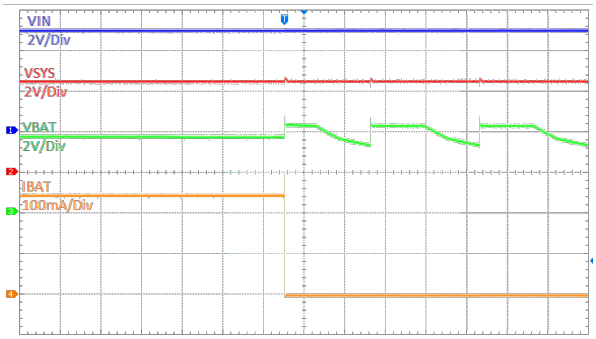
VIN Un-Plug, Charge Stop Waveform

CH1 = VIN, CH2 = VSYS, CH3 = ISYS,
CH4 = IBAT



Battery Removal

CH1 = VIN, CH2 = VSYS, CH3 = ISYS,
CH4 = IBAT



OPERATION

General Description

The ETA4098 is a single cell battery charger with power path management function for Li-Ion and Li-Polymer battery. It features pre-charging, fast charging (CC) and constant voltage (CV) charging, end-of charging termination, and auto-recharge.

A bypass FET between IN and SYS pins, and a battery switch FET between SYS and BAT pins are integrated for providing complete power path management. System load is prior in getting power from the input or is switched to battery power when the input is weak or is removed. Power to the battery is regulated by the battery switch FET during charging, while the input voltage, input current, voltage to system load, chip temperature.

Figure 1: shows the power paths and key circuit blocks in the ETA4098, where the Qbypass regulates voltage to the system load and to the circuit for charging, the Qrvs prevents reverse leakage from the SYS node to IN node and the Qswitch regulates for charging or gates the discharging from the BAT node to SYS node. The charging circuit and the discharging have their own UVLO and bias, and the common circuit is powered by the higher voltage of the IN node or SYS node. The I/F is ready whenever any power is available.

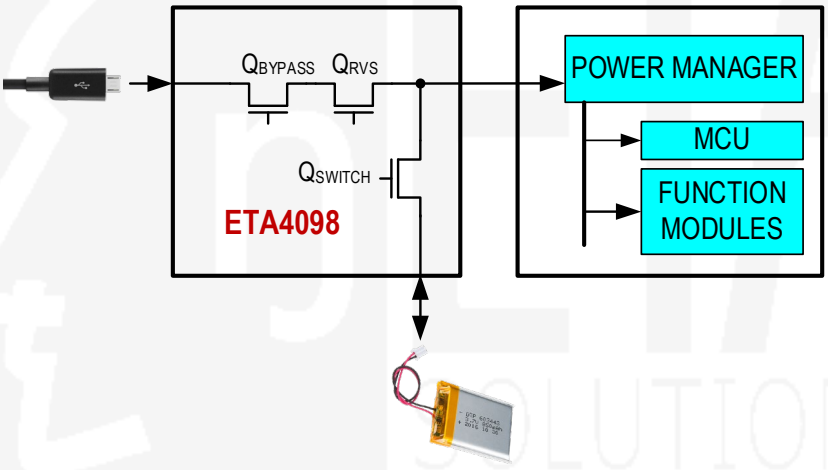


Figure 1: Power Path Management Structure

Input Detection

The device monitors the input at the IN node. When the input is within the normal range certified by the UVLO circuit and OVP circuit for more than t_{INI} the charge circuit starts. The circuit stops or turns into OVP cut off instantly when the input voltage is lower than VIN_UVLO or is higher than VIN_OVLO, that the Qbypass and Qrvs are turned open.

Figure 2: shows the timings relative to the input detection. The input state is certified after t_{INI} and stays for over t_{PWD}, the device outputs a pulse through the nINT. The nINT is internally pulled up to an unregulated reference voltage unless the battery is set into disconnected state. The nINT asserts pulse whenever an effective input change is certified, while the changes occurring within t_{PWM} do not assert pulse.

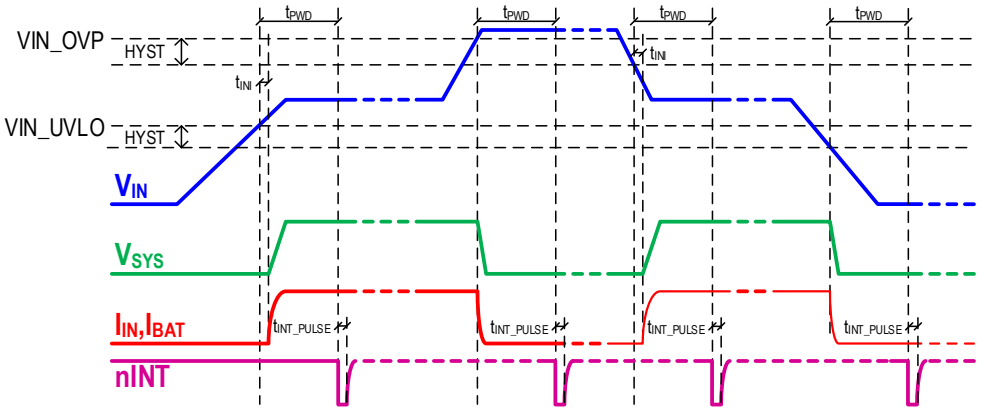


Figure 2: Input Power Detection and Operation Timings

Power Path Management

When the input is available (V_{IN} > V_{IN_UVLO}, V_{IN} - V_{SYS} > V_{HDRM}), the device intends to power the system load with input by regulating the input voltage to V_{SYS_REG} (V_{SYS} is decided by the input voltage, input current limit and battery voltage in reality).

Battery Charge Profile

The charging profile managed by the device is as shown in *Figure 3*, which is segmented as following phases:

Pre-charge: If the battery voltage is less than the pre-charging threshold V_{BAT_PRE}, it charges the battery with pre-charging current, which shares the same value of the termination current programmed by IEOC resistor.

Constant-Current Charge: When battery voltage is higher than V_{BAT_PRE}, and is less than V_{BAT_REG}, it is charged with constant current that is programmed by the resistor connected to GND from ISET pin.

Table 1. Charge Current Configuration by ISET Resistor

ISET RESISTOR (kΩ)	CHARGE CURRENT (mA)
1	800
1.5	533.3333
1.8	444.4444
2	400
3.2	250
4.7	170.2128
5	160
8	100
10	80

Constant-Voltage Charge: When the battery voltage rises close to the battery voltage V_{BAT_REG} = 4.2V, the charge current begins to decreases until the termination situation is identified.

During the whole charging process, the actual charge current may be less than the register setting due to other loop regulations like dynamic power management (DPM) regulation (input voltage, input current), or thermal regulation.

Table 2. Termination Charge Current Configuration by IEOC Resistor

IEOC RESISTOR (kΩ)	TERMINATION CHARGE THRESHOLD (mA)
2	125
4	62.5
5	50
8	31.25
10	25
20	12.5
50	5

A new charge cycle starts when the following conditions are valid:

- The input power is recycled, or
- Auto-recharge kicks in.

Under the following conditions:

- No battery over voltage event.

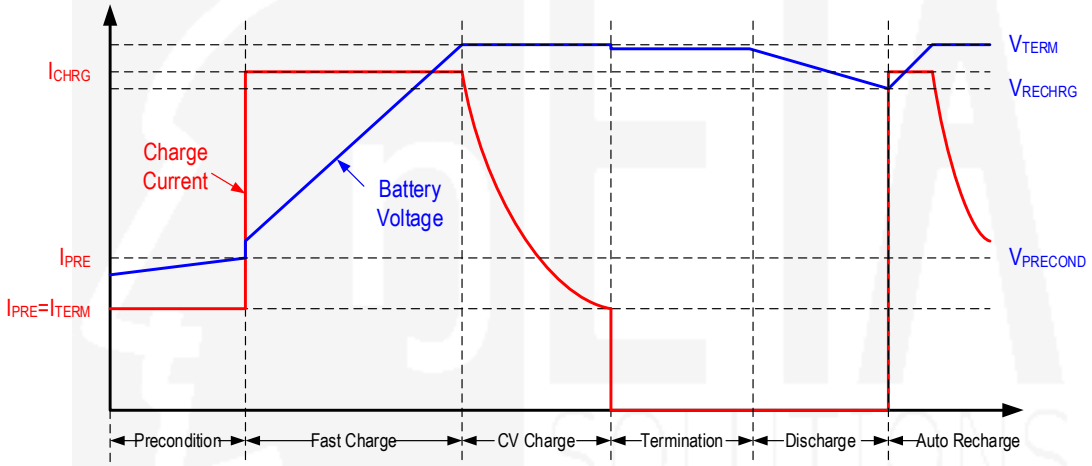


Figure 3: Battery Charge Profile

Battery Over-Voltage Protection

This device is designed with a built-in battery over-voltage limit about V_{BAT_OVP} higher than the V_{BAT_REG}. When the battery over-voltage event occurs, the device immediately suspends the charging and asserts a fault. A discharging path is turned on when the battery OVP keeps.

Input Current and Input Voltage Based Power Management

To meet the input source (USB usually) maximum current limit specification, the IC features the input current based power management by continuously monitoring the input current. The total input current limit is fixed at 500mA prevent the input source from over-loaded.

If the preset input current limit is higher than the rating of the input source, the back-up input voltage based power management also works to prevent the input source from being over-loaded. Either the input current limit or the input voltage limit is reached, the Qbypass between IN and SYS pins will be regulated so that the

total input power will be limited. As a result the system voltage drops, once the system declines to minimum value of the V_{SYS_REG} - D_{VSYS_LOW} and V_{IN} - D_{VIN_LOW}, the charge current will be reduced to prevent the system voltage from dropping further.

The voltage based dynamic power management (DPM) will regulate the input voltage to V_{IN_MIN} when the load is over the input power capacity.

The V_{IN_MIN} is fixed at 4.6V.

Battery Supplement Mode

As mentioned above, the charge current is reduced to keep the input current or input voltage in regulation when DPM happens. If the charge current is reduced to zero and the input source is still overloaded due to heavy system load, the system voltage starts to decrease. Once the system voltage falls D_{VSYS}-BAT_LOW below the battery voltage, the device enters battery supplement mode and the ideal diode mode will be enabled. The Qswitch is regulated to maintain the V_{BAT} - V_{SYS} at D_{VSYS}-V_{BAT_REG} when I_{DSCHG} (supplement current) × R_{ON_BAT} is lower than D_{VSYS}-V_{BAT_REG}, in the case the I_{DSCHG}×R_{ON_BAT} is higher than D_{VSYS}-V_{BAT_REG}, the Qswitch is fully turned on to keep ideal forward voltage. During system load decreasing, once V_{SYS} is higher than V_{BAT} + D_{VSYS}-BAT_HIGH, the ideal diode mode will be disabled. Figure 4 shows the dynamic power management and battery supplement mode operation profile.

When VIN is not available, the device operates in discharge mode; the Qswitch is always fully on to reduce the loss.

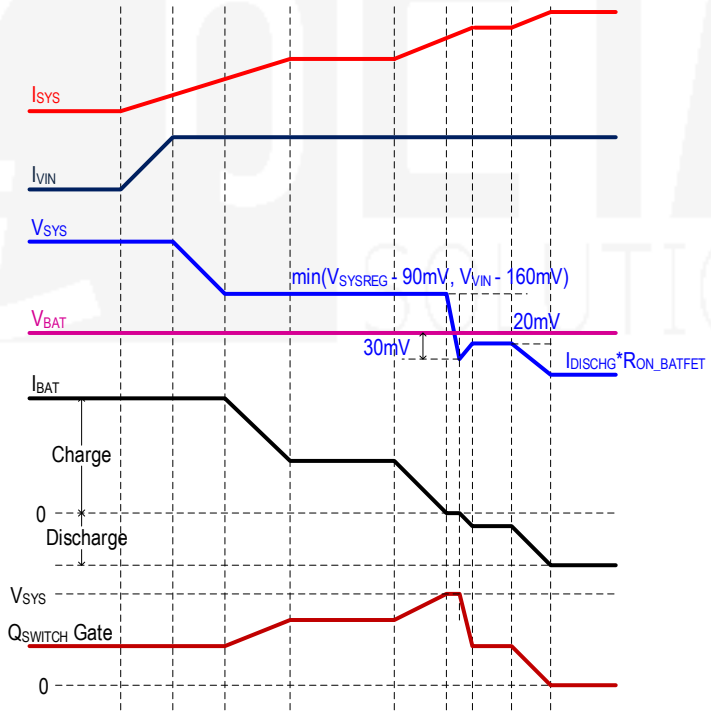


Figure 4: Dynamic Power Management and Battery Supplement Operation Profile

Battery Regulation Voltage

The battery voltage for the constant voltage regulation phase is V_{BAT_REG}. When battery is float, the BAT pin voltage varies between V_{BAT_REG} - V_{RECH} and V_{BAT_REG}.

Thermal Regulation and Shutdown

The device continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches preset limit of T_{J_REG}, the device starts to reduce the charge current to prevent higher power dissipation

When the junction temperature reaches T_{J_SHDN} that is slightly higher than most high programmable thermal regulation temperature threshold, both the Qbypass and Qswitch are turned off.

nSTAT Charging Status

Table 3. nSTAT Indication

STATE	nSTAT BEHAVIOUS
- Precondition State, or - Fast Charge State, or - Constant Voltage State	nSTAT is pulled low.
- Charge Disable, or - Charge Done State	nSTAT is floating
- Charge Fault State	nSTAT is driven ON(0.5s)/OFF(0.5s)

Battery Discharge Function

If battery is connected and the input source is missing, the BETFET is fully on when V_{BAT} is above the V_{BAT_UVLO} threshold. The low Ron Qswitch minimizes the conduction loss during discharge. The quiescent current of the device is as low as 6μA in this mode.

Over-Discharge Current Protection

The over-discharge current protection is effective in discharge mode and supplement mode. Once the I_{BAT} exceeds discharge current limit, fixed at 2A, the Qswitch cuts off after t_{DSCHG_CUT} and the device resumes conducting after t_{RETRY}. Besides, if the discharge current goes high to hit I_{DSCHG_S}, the Qswitch cuts off instantly.

When the battery voltage falls below V_{BAT_UVLO}, the Qswitch cuts off to prevent over discharge.

System Short Circuit Protection

When system short circuit occurs, the Qswitch cuts the BAT to VSYS path and the Qbypass limits the current input through the VIN to SYS path. If the system short circuit remains, the die temperature goes high to cause thermal shut down.

The ETA4098 features VSYS node short circuit protection for both VIN to VSYS path and BAT to VSYS path.

- ***VIN to VSYS path:*** The ETA4098 starts activate hard short protection after V_{SYS} goes greater than 1.5V once. This means the IC allows to start-up with full current limit. Once this condition occurs, if V_{SYS} falls below 1.5V, and I_{IN} is found over the protection threshold, Q_{SWITCH}, Q_{BYPASS} and Q_{RVS} are turned off immediately. And the operation of the IC goes into the hiccup mode. Beside hard short protection, at any time V_{SYS} is lower than 1.5V, while the setting input current limit is reached, I_{IN} is regulated at I_{IN_LIM} the hiccup mode also starts after a 60μs delay. The interval of the hiccup mode is 800us.
- ***BATT to SYS path:*** Once I_{BAT} is found over the 3.7A protection threshold, both the LDO FET and the BATT FET are turned off immediately and the operation of the IC goes into the hiccup mode. Besides, while the battery discharge current limit threshold is reached, the hiccup mode also starts after a 60μs delay. The interval of the hiccup mode is 800us. For details, please refer to flow chart in Figure 7.
- Particularly, if the system short circuit happens when both input and battery are present, the protection mechanism of both paths will work, the faster one dominates the hiccup operation.

Interrupt to Host (INT)

This device also has an alert mechanism which can output an interrupt signal via nINT pin to notify the system on the operation by outputting low for t_{INT_PULSE}. Any of the events listed below triggers the nINT output.

- Good input source detected
- UVLO or input over voltage detected
- Charge completed
- Charging status change
- Any fault (input fault, battery OVP fault)

The nINT is pulled up to an unregulated low voltage that is not high enough to most logic circuit (in the circuit the device loads), to avoid unexpected creeping powering and leakage during power recycling and in shipping mode; the nINT is pulled up to a high voltage in other states. Both the low voltage and high voltage are internally generated and pull up is weak and could be over-driven externally.

Battery Disconnection Function

This device can also reuses nINT pin to cut off the path from battery to system under the condition need to recycle the system power. Once the logic at nINT pin set to low for more than t_{INT_OFF} which can be programmed via t_{RST_DGL}, the battery is disconnected from the system by turning off the Qswitch and Qbypass, the off state lasts for t_{INT_ON} which can be programmed via t_{RST_DUR}, then the Qswitch and Qbypass will be automatically turned on and system is powered again. During the off period, the nINT pin is biased to a lower voltage.

The waveforms of power recycling are shown in *Figure 5.*

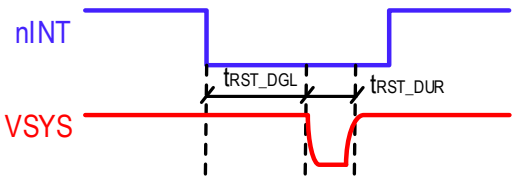


Figure 5. Power Recycling Waveforms

OPERATION DIAGRAM

Main State Machine

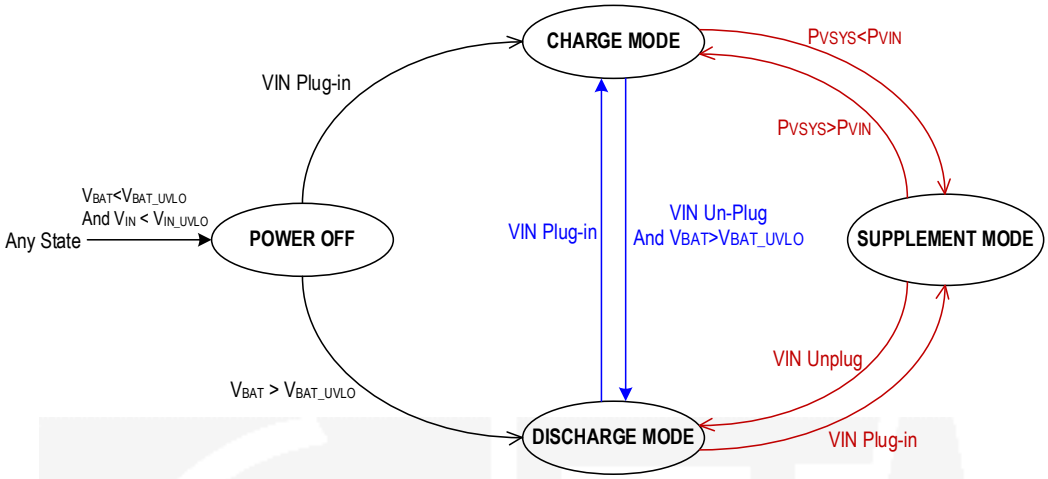


Figure 6: State Machine Conversion

Charger Flow Chart

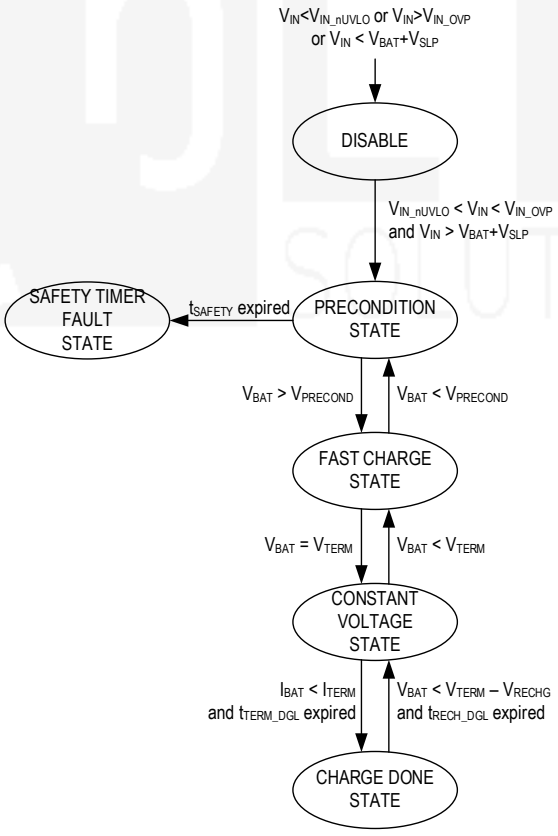


Figure 7: Charger Flow Chart

System Short Circuit Protection

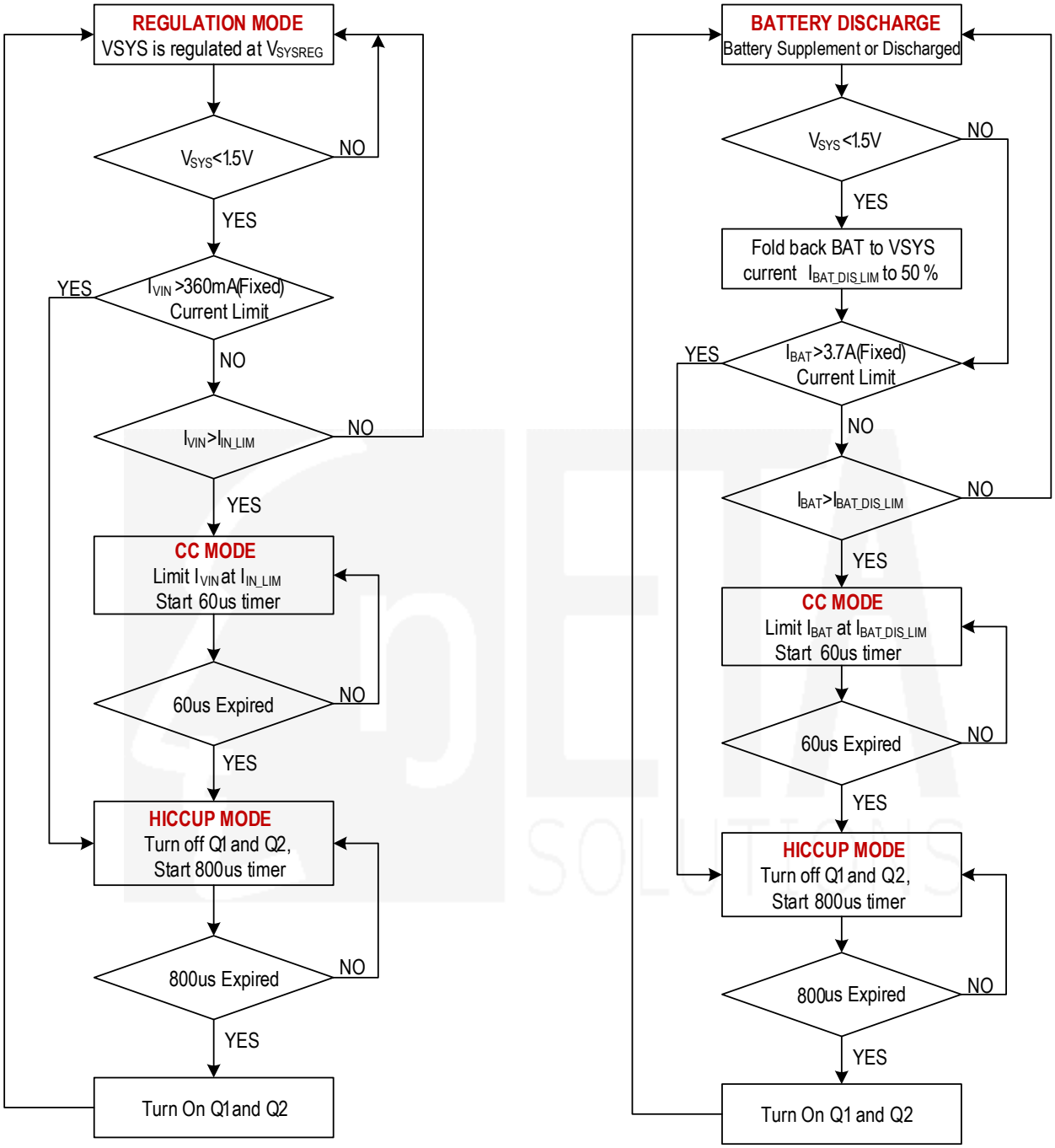


Figure 8: System Short Circuit Protection

APPLICATION INFORMATION

Input Capacitor

An input capacitor is required for stability, at least, a 1μF capacitor has to be connected between IN to GND for stable operation over full load current range. Basically, it is OK to have more output capacitance than input, as long as the input is at least 1μF.

Output Capacitor

This device is designed specifically to work with a very small ceramic output capacitor. A ceramic capacitor (dielectric types X5R or X7R) >2.2μF is suitable in the ETA4098 application circuit. For this device, the output capacitor should be connected between VSYS pin and GND pin with thick trace and small loop area.

BAT to GND Capacitor

The capacitor from the BAT pin to GND pin is also necessary for ETA4098. A ceramic capacitor (dielectric types X5R or X7R) >2.2μF is suitable for the ETA4098 application circuit.

VDD to GND Capacitor

The capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

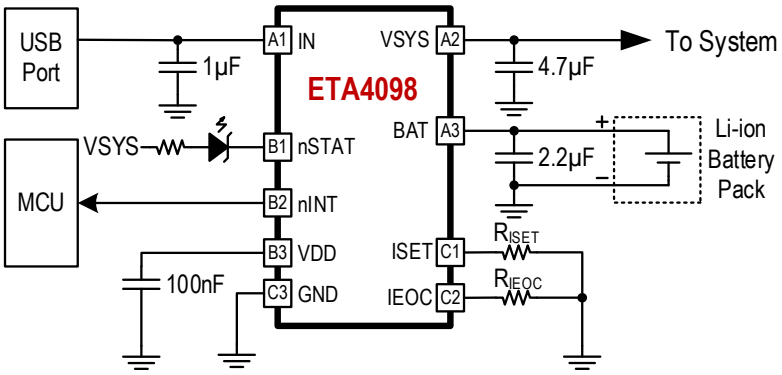
PCB Layout Guideline

Put external capacitors as close to this device as possible to make sure the smallest input inductance and the ground impedance.

The PCB trace to connect the capacitor between VDD and GND is very important, and it should be put very close to this device.

The GND for the I2C wire should be clean, and it should not be very close to the GND.

EVALUATION KIT DESIGN



Note: Pin# for QFNFC package

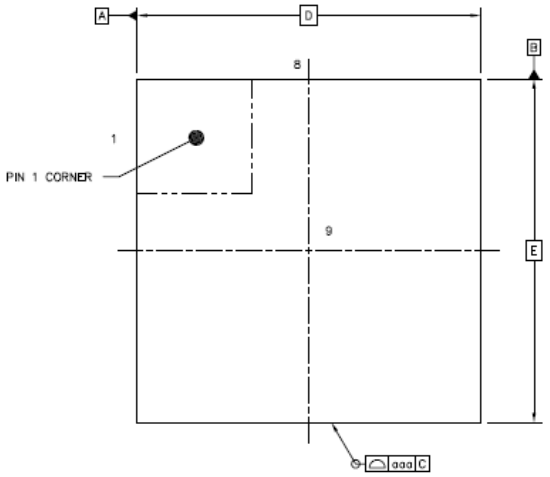
Figure 9: ETA4098 EVKIT Design

Table 4: ETA4098 EVKIT BOM List

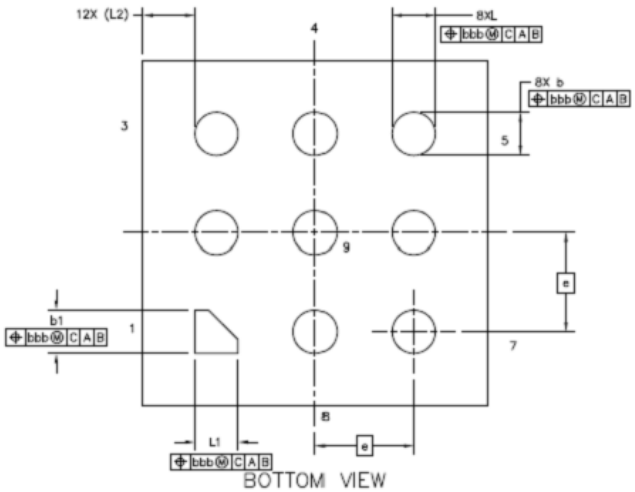
QTY	DEVICE	VALUE	DESCRIPTION	PACKAGE	RECOMMENDED MANUFATURE
1	C1	1µF	20V Ceramic Capacitor (X5R or X7R)	0603	TBD
2	C2, C4	2.2µF	10V Ceramic Capacitor (X5R or X7R)	0603	TBD
2	C3, C5	4.7µF	10V Ceramic Capacitor (X5R or X7R)	0603	TBD
1	C6	100nF	10V Ceramic Capacitor (X5R or X7R)	0603	TBD
4	R1, R2, R3, R4	15kΩ	Resistor	0603	TBD
1	PB		Push Button		TBD

PACKAGE OUTLINE DIMENSIONS

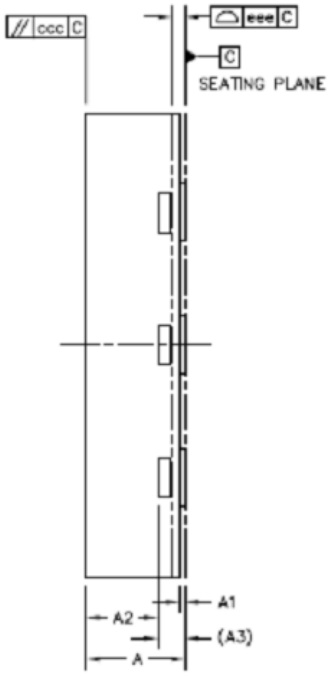
Package: FCQFN-9L 1.75mmx1.75mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.32	0.37	0.4
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.27	---
L/F THICKNESS		A3		0.102 REF	
LEAD WIDTH		b	0.17	0.22	0.27
		b1	0.12	0.22	0.32
BODY SIZE	X	D		1.75 BSC	
	Y	E		1.75 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.17	0.22	0.27
		L1	0.12	0.22	0.32
LEAD EDGE TO PACKAGE EDGE		L2		0.265 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	