360nA Ultra-low Iq, COT Synchronous Buck Converter

DESCRIPTION

The ETA3707/A is a high-efficiency, DC-to-DC step-down switching regulator that features 360nA ultra-low quiescent current. ETA3707 can provide output voltages from 1.2V to 3.3V, which is capable of delivering up to 1A of output current. ETA3707A can provide output voltages from 0.7V to 3.1V, which is capable of delivering up to 500mA of output current. ETA3707/A adopts an adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load. During light load, ETA3707/A goes into a PFM mode that saves switching loss to achieve high efficiency. The adaptive COT control also maintains a constant switching frequency across line and load. The internal soft-start control circuitry reduces inrush current. Over current and temperature protection improve design reliability.

ETA3707/A is available in a tiny CSP-8 and DFN2x2-8 package.

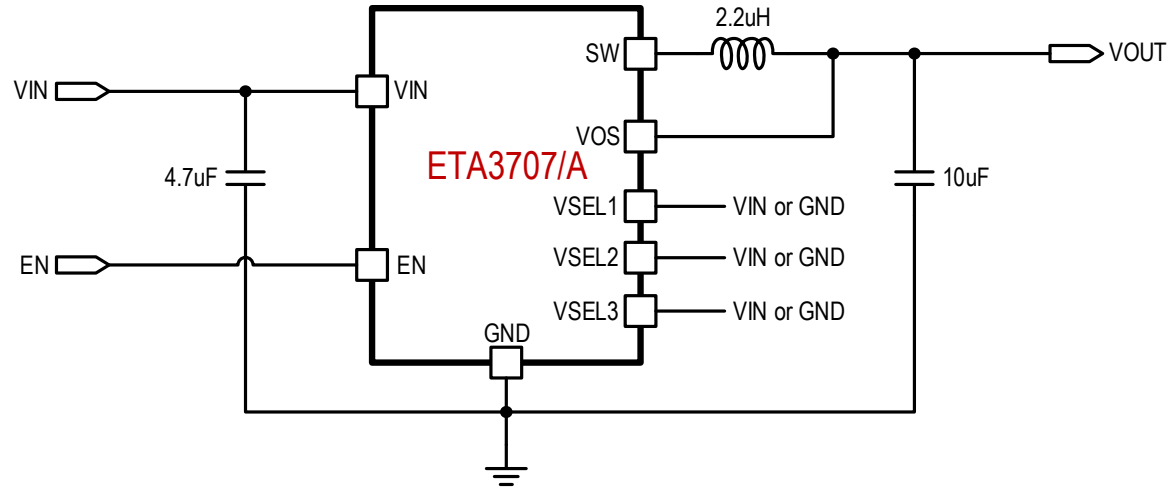
FEATURES

- Input Voltage Range: 2.1V to 5.5V
- 360nA Quiescent Current
- Programmable Output Voltage
  - ETA3707: 1.2V to 3.3V
  - ETA3707A: 0.7V to 3.1V
- Output Current
  - ETA3707: 1A Max
  - ETA3707A: 500mA Max
- Adaptive COT Control
- Ultra-fast Load Transient Response
- 1.2MHz Switching Frequency
- High Efficiency PFM Mode at Light Load
- Over Current Protection
- Over Temperature Protection
- Available in CSP-8 and DFN2x2-8 Package
- RoHS Compliant

APPLICATIONS

- Wearable
- IoT
- Battery-Powered Devices

TYPICAL APPLICATION

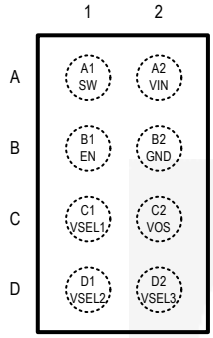


ORDERING INFORMATION

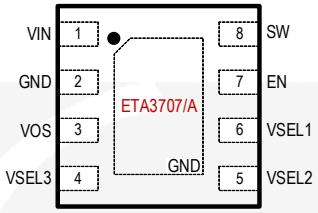
PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA3707CSI	CSP-8	3707 YWWL	3000
ETA3707ACSI	CSP-8	3707A YWWL	3000
ETA3707D2I	DFN2x2-8	CZYW	3000
ETA3707AD2I	DFN2x2-8	CaYW	3000

PIN CONFIGURATION

Top View



CSP-8



DFN2x2-8

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN, SW, EN, VOS to GND Voltage ..... –0.3V to 6V
VSEL1,VSEL2,VSEL3 to GND Voltage ..... –0.3V to 6V
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C

Thermal Resistance	Θ_{JA}	Θ_{JC}	
DFN2x2-8	75	20	°C/W
CSP-8	118.5		°C/W

Lead Temperature (Soldering 10sec) .....260°C
ESD HBM (Human Body Mode) 3KV
ESD CDM (Charged Device Mode) 1KV

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.1		5.5	V
Input UVLO	Rising, Hysteresis=200mV		2	2.15	V
Input Supply Current	No switching		360	1000	nA
Input Shutdown Current			0	1	μA
Output Voltage Accuracy	V_{OUT}=1.8V,I_{OUT}=10mA	-2.5		2.5	%
	V_{OUT}=1.8V,I_{OUT}=100mA	-2		2	%
Load Regulation	PFM to PWM, V_{OUT}=1.8V		0.002		%/mA
	Only PWM, V_{OUT}=1.8V		0.0005		%/mA
Line Regulation	V_{IN}=2V to 5.5V, V_{OUT}=1.8V		0.1		%/V
Switching Frequency			1.2		MHz
Soft Start Time	V_{OUT} rise from 10% to 90%		0.5		mS
100% Duty Threshold	V_{IN} Rising, Exiting 100% V_{IN}=V_{OUT}+V_{TH_100+}		250		mV
	V_{IN} Failing, Entering 100% V_{IN}=V_{OUT}+V_{TH_100-}		200		

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
High Side Switch On Resistance			200		mΩ
Low Side Switch On Resistance			190		mΩ
High Side Current Limit			1.5		A
Low Side Current Limit			1		A
SW Leakage Current	V_{OUT}=5.5V, V_{SW}=0 or 5.5V, EN= GND		0	0.1	μA
VOS Input Leakage Current	V_{OUT}=2V,EN=V_{IN}		100		nA
Output Discharge Resistance	EN=GND		10		Ω
EN,VSEL1,VSEL2.VSEL3 Logic High Threshold	Rising	1.2			V
EN,VSEL1,VSEL2.VSEL3 Logic Low Threshold	Falling			0.4	V
EN,VSEL1,VSEL2.VSEL3 Input Bias Current	V_{EN}=2V		10		nA
Thermal Shutdown	Rising, Hysteresis =34°C		150		°C

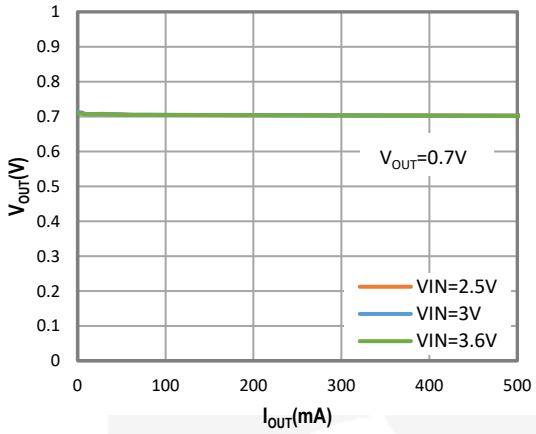
PIN DESCRIPTION

CSP-8 PIN #	DFN2x2-8 PIN #	NAME	DESCRIPTION
A1	8	SW	Inductor connection pin. Connect an inductor between SW and the regulator output.
A2	1	VIN	Supply voltage pin. Bypass with a 4.7μF ceramic capacitor to GND.
B1	7	EN	Enable pin for the IC. Drive this pin high to enable the IC, low to disable. This pin must be terminated.
B2	2	GND	Ground.
C1	6	VSEL1	Output voltage selection pin. This pin must be terminated.
C2	3	VOS	Output pin. Bypass with a 10uF or larger ceramic capacitor closely between this pin and GND.
D1	5	VSEL2	Output voltage selection pin. This pin must be terminated.
D2	4	VSEL3	Output voltage selection pin. This pin must be terminated.

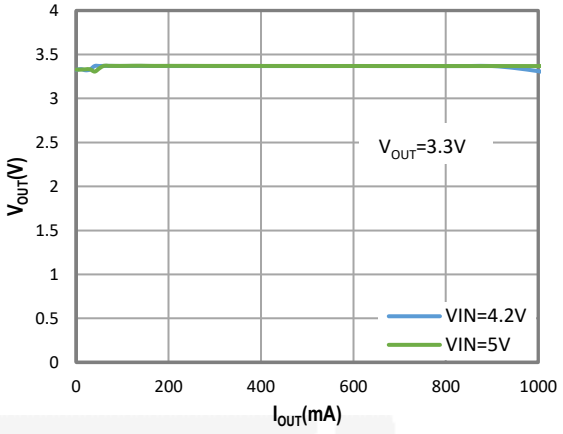
TYPICAL CHARACTERISTICS

(Typical values are at T_A = 25°C unless otherwise specified.)

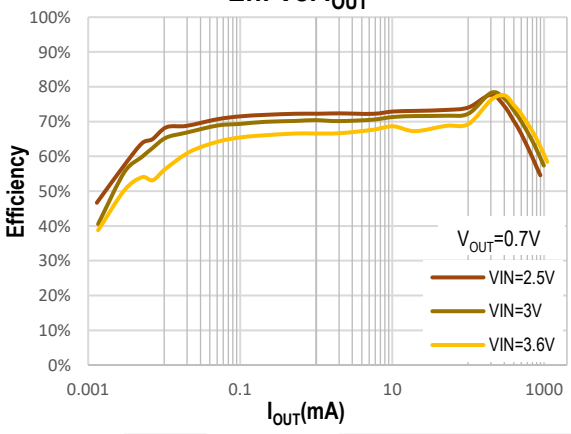
V_{OUT} Vs. I_{OUT}



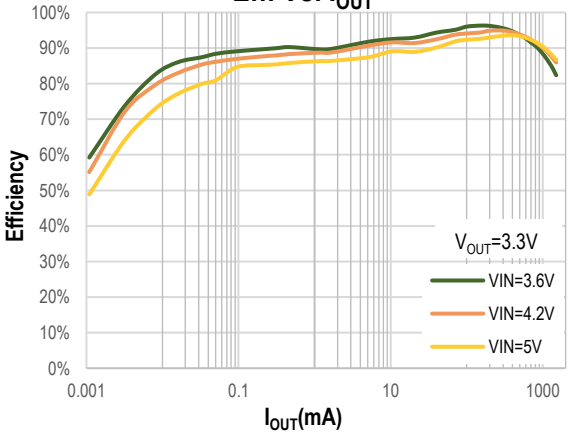
V_{OUT} Vs. I_{OUT}



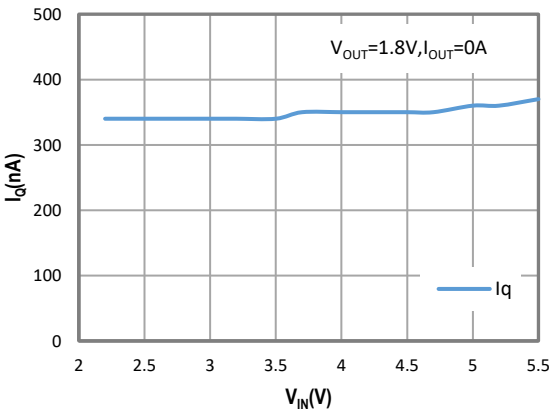
Eff. Vs. I_{OUT}



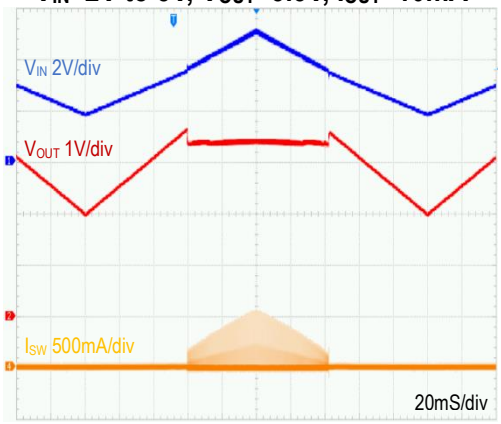
Eff. Vs. I_{OUT}



I_Q Vs. V_{IN}



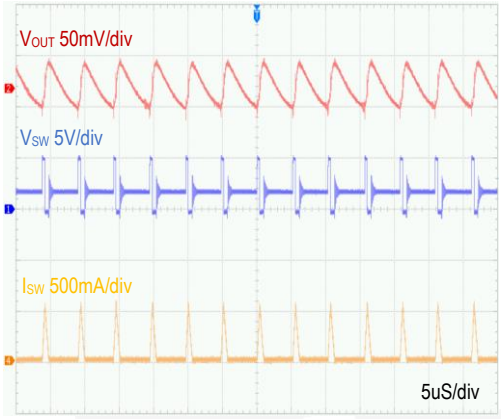
100% Duty Cycle Entry and Leave Operation
V_{IN}=2V to 5V, V_{OUT}=3.3V, I_{OUT}=10mA



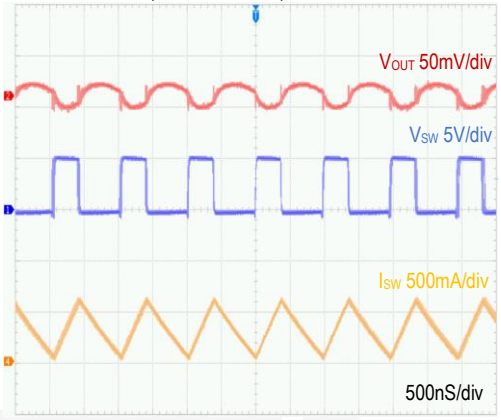
TYPICAL CHARACTERISTICS Cont'd

(Typical values are at T_A = 25°C unless otherwise specified.)

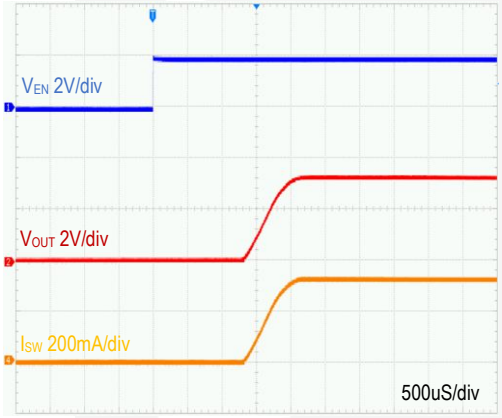
Output Voltage Ripple
V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=50mA



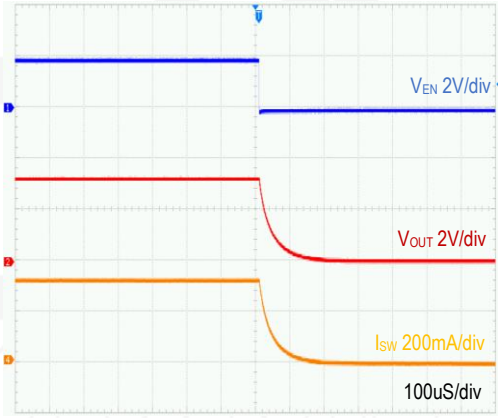
Output Voltage Ripple
V_{IN}=5V,V_{OUT}=1.8V,I_{OUT}=300mA



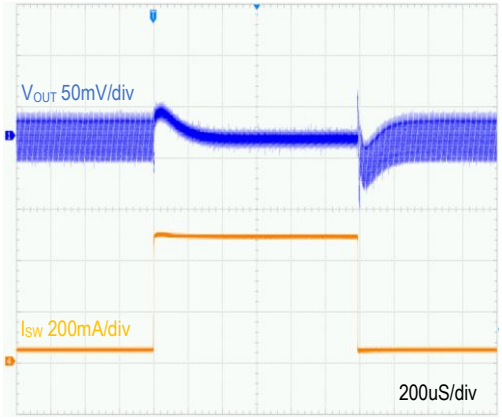
Start Up from EN
V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=300mA



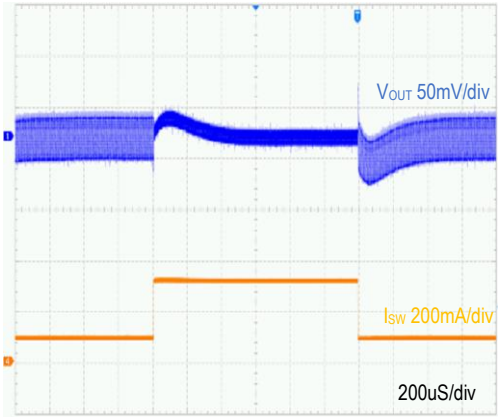
Shut Down from EN
V_{IN}=3.6V, V_{OUT}=3.3V, I_{OUT}=300mA



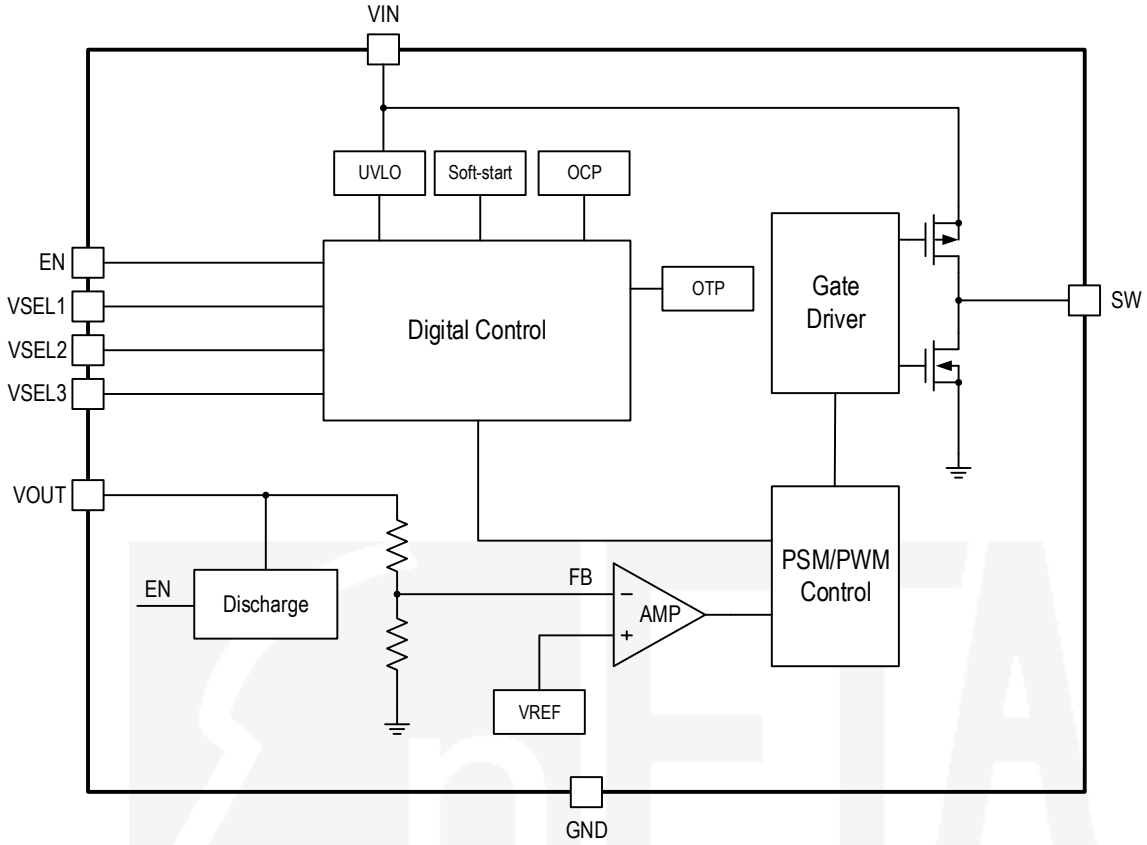
Load Transient Response
V_{IN}=5V, V_{OUT}=1.8V,I_{OUT}=50-500mA



Load Transient Response
V_{IN}=5V, V_{OUT}=3.3V,I_{OUT}=100-300mA



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ETA3707/A is a high-efficiency and high-frequency DC-to-DC step-down switching regulator, capable of delivering up to 1A(ETA3707) or 500mA(ETA3707A) of output current. It adopts an adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load. It compares the sum of the FB voltage and a ripple voltage that mimics the voltage due to the output ESR and capacitance. The constant-on-time timer varies with line to achieve relative constant switching frequency across line.

Light Load Operation

Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFET, power is lost due to the finite Rdson of the MOSFET and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. ETA3707/A goes into a power save mode during light load, thereby extending the range of high efficiency operation.

100% Duty Cycle Operation

If the input voltage decreases and the difference voltage between input and output is lower than VTH_100-, ETA3707/A will enter 100% duty cycle operation, and the output voltage follows the input voltage minus the voltage drop across the internal PMOSFET and the inductor. Once the input voltage increases and trips the threshold VTH_100+, the IC will exit 100% duty cycle operation to switch normally.

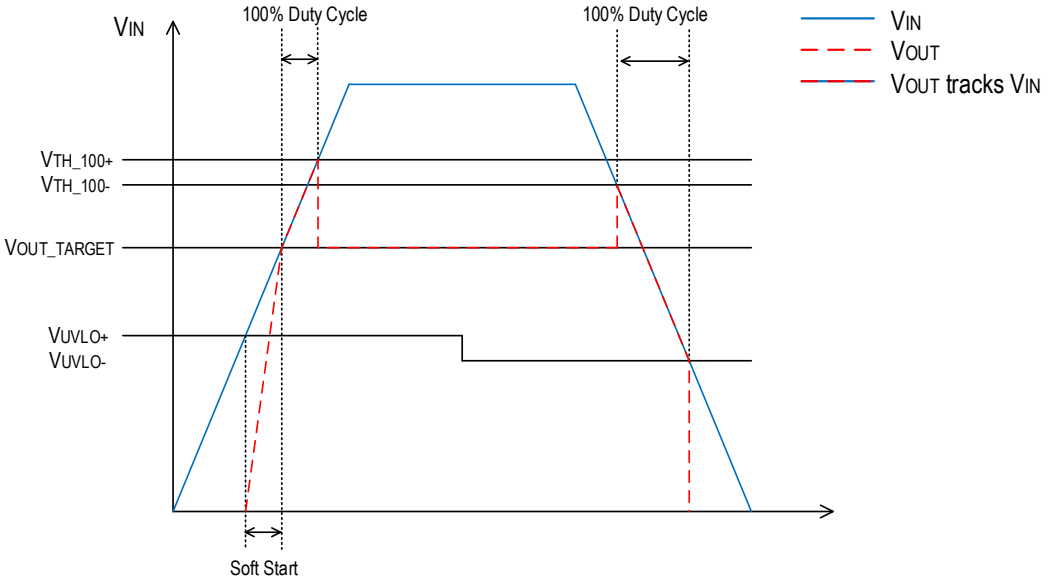


Figure 1. 100% Duty Cycle Entry and Leave Operation

Output Voltage Selection

The output voltage of ETA3707/A can be programmed by the three pins VSEL1, VSEL2 andVSEL3. To set the output voltage, please refer to the table below.

Table1. Output Voltage Setting

Device	VOUT(V)	VSEL3	VSEL2	VSEL1
ETA3707	1.2	0	0	0
	1.5	0	0	1
	1.8	0	1	0
	2.1	0	1	1
	2.5	1	0	0
	2.8	1	0	1
	3	1	1	0
	3.3	1	1	1
ETA3707A	0.7	0	0	0
	1	0	0	1
	1.3	0	1	0
	1.6	0	1	1
	1.9	1	0	0
	2	1	0	1
	2.9	1	1	0
	3.1	1	1	1

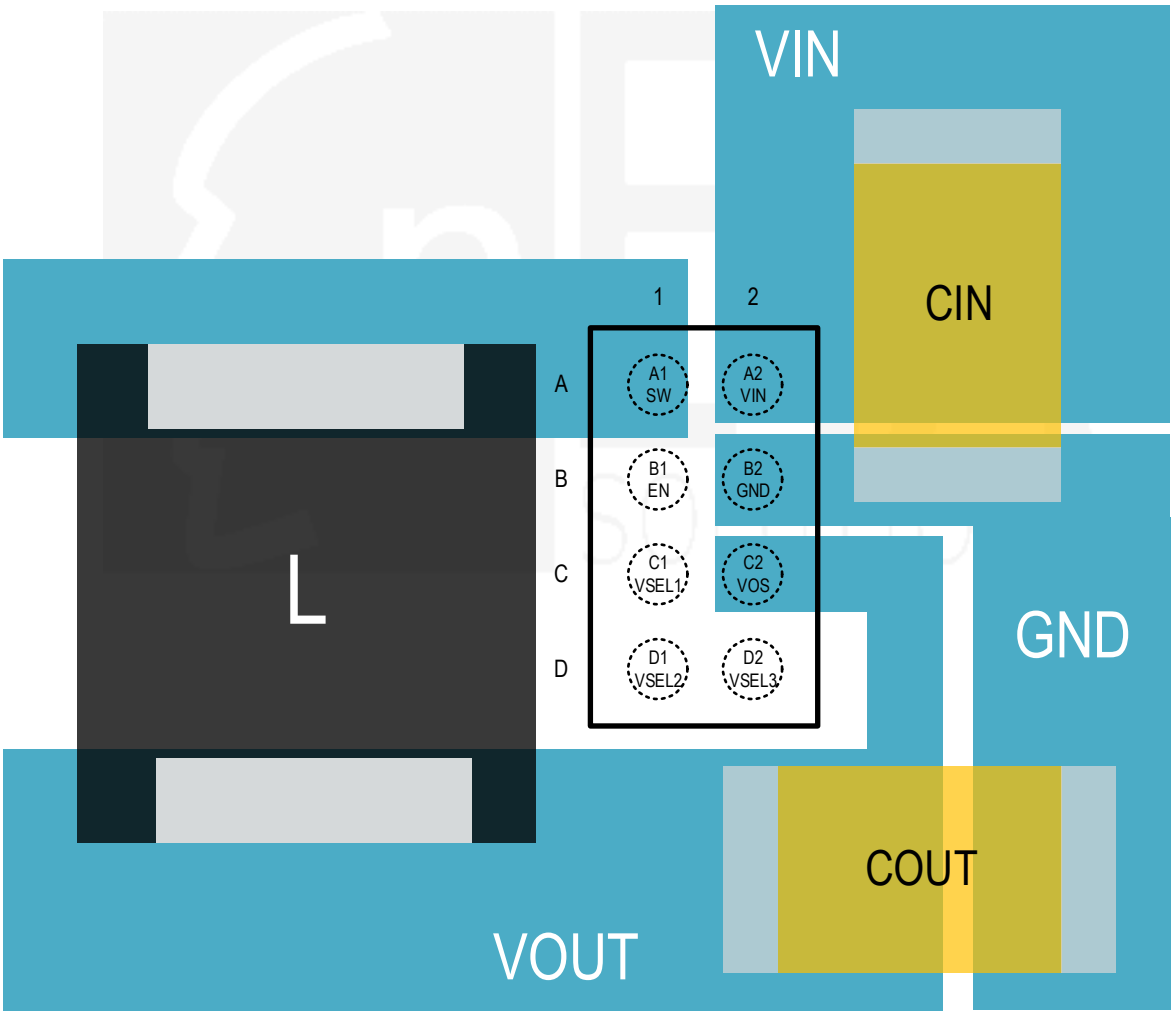
Over-Temperature Protection

Thermal protection disables the output when the junction temperature rises to approximately 150°C, allowing the device to cool down. When the junction temperature cools to approximately 115°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

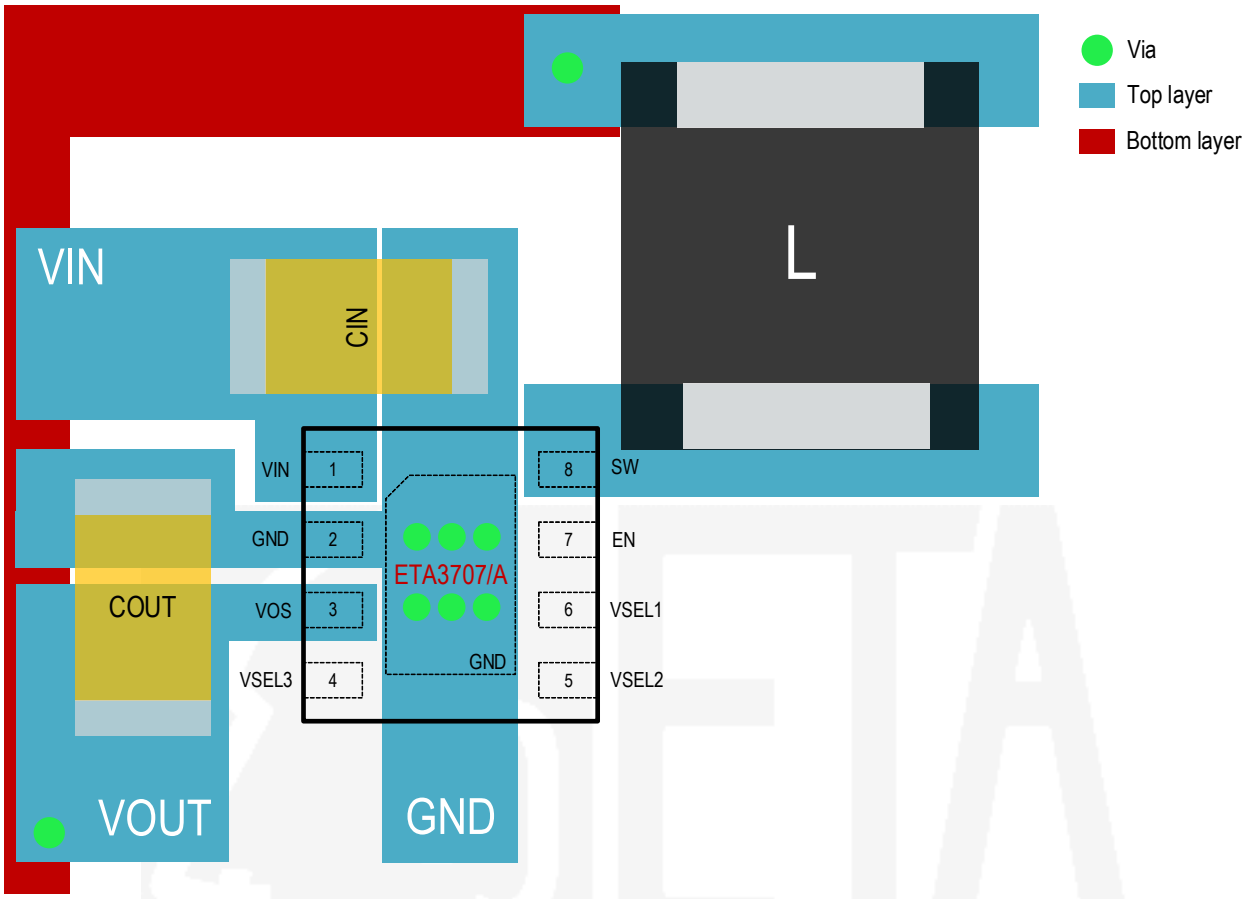
PCB LAYOUT GUIDE

Keep the power devices as close to the chip as possible to achieve the smallest power loop area, which leads to the best EMI performance; CIN is always placed nearest to VIN and GND.

Package: CSP-8

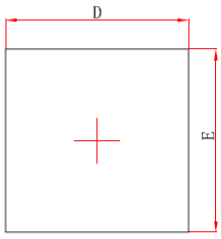


Package: DFN2x2-8

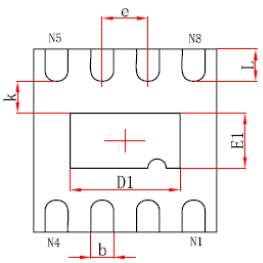


PACKAGE OUTLINE

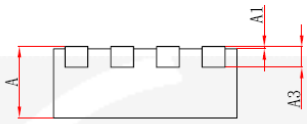
Package: DFN2x2-8



Top View

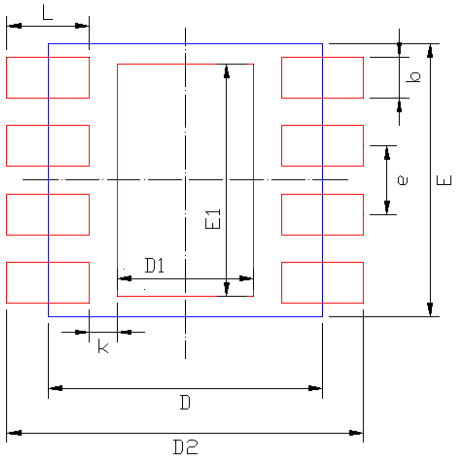


Bottom View



Side View

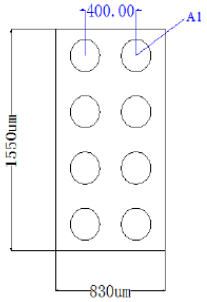
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	1.100	1.300	0.043	0.051
E1	0.500	0.700	0.020	0.028
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.274	0.426	0.011	0.017



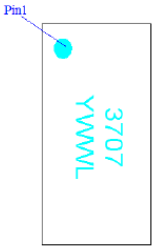
DFN2X2-8

Dimensions	Value (in mm)
D	2
E	2
D1	1
E1	1.7
D2	2.6
e	0.5
b	0.3
k	0.2（≥0.2）
L	0.6

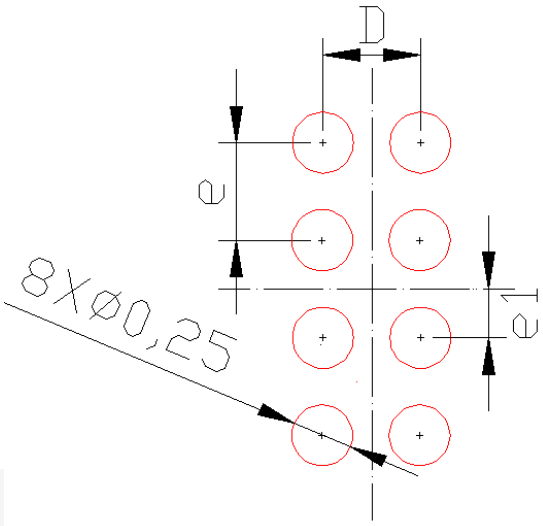
Package: CSP-8



Bottom View



Top View



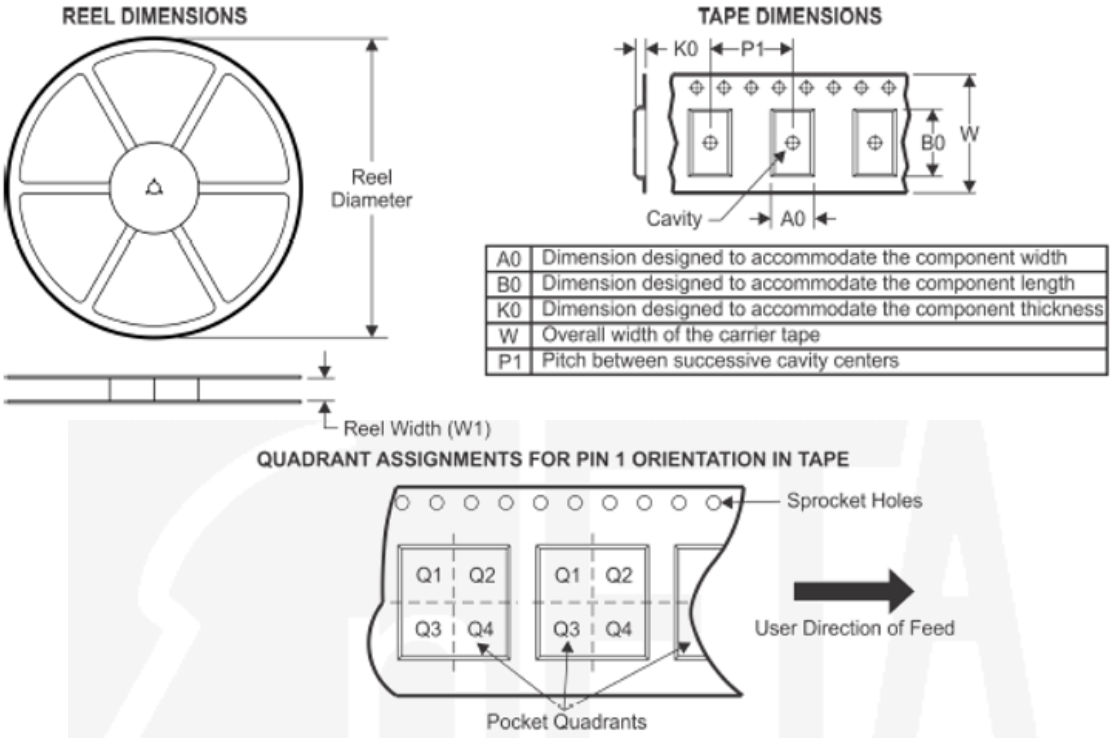
CSP-8

Side view

Dimensions	Value (in mm)
D	0.4
e	0.4
e1	0.2
Φ	0.25

Parameter	Min	Normal	Max
	Millimeters		
Package body dimension X	0.81	0.83	0.85
Package body dimension Y	1.53	1.55	1.57
Package Height	0.52	0.55	0.58
SI thickness	0.3125	0.325	0.34
Bump Height	0.18	0.2	0.22
Bump Diameter	0.25	0.27	0.29
Total Ball Count Per Die	/	8	/
Ball Pitch X axis (min)	/	0.4	/
Ball Pitch Y axis (min)	/	0.4	/

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA3707CSI	CSP-8	8	3000	178	9.5	0.91	1.76	0.68	4	8	Q1
ETA3707ACSI	CSP-8	8	3000	178	9.5	0.91	1.76	0.68	4	8	Q1
ETA3707D2I	DFN2x2-8	8	3000	180	9.5	2.3	2.3	1.1	4	8	Q1
ETA3707AD2I	DFN2x2-8	8	3000	180	9.5	2.3	2.3	1.1	4	8	Q1