1.5A, 3MHz Step-Down Converter in SOT23-5 Package

DESCRIPTION

The ETA3424 is a high-efficiency, DC-to-DC step-down switching regulator, work in forced PWM mode, capable of delivering up to 1.5A of output current. The devices operate with an input voltage range from 2.6V to 7V and provide fixed output voltages of 1.2V, 2.5V and 3.3V, making the ETA3424 ideal for low voltage power conversions. Running at a fixed frequency of 3MHz allows the use of small inductance value and low DCR inductors, thereby achieving higher efficiencies. Other external components, such as ceramic input and output caps, can also be small due to higher switching frequency, while maintaining exceptional low noise output voltages. Built-in EMI reduction circuitry makes this converter ideal power supply for RF applications. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

ETA3424 is housed in a tiny SOT23-5 package.

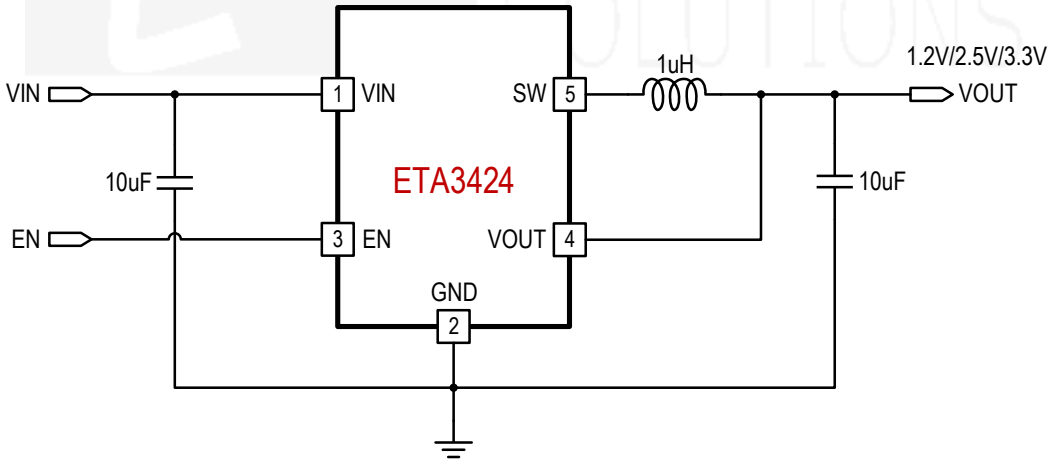
FEATURES

- Up to 96% Efficiency
- Fixed Output Voltage:1.2V/2.5V/3.3V
- Up to 1.5A Max Output Current
- 3MHz Switching Frequency
- Forced PWM Mode
- Internal Compensation
- Tiny SOT23-5 Package
- RoHS Compliant

APPLICATIONS

- LCD TV
- Set Top Box
- IP CAM

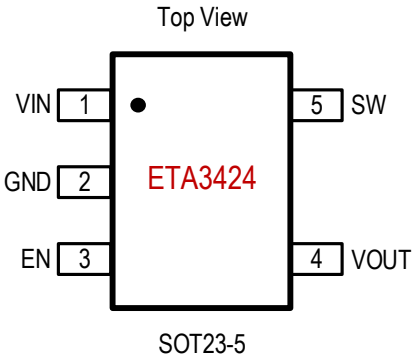
TYPICAL APPLICATION



ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA3424V12S2F	SOT23-5	IvYW	3000
ETA3424V25S2F	SOT23-5	IF|YW	3000
ETA3424V33S2F	SOT23-5	IP|YW	3000

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN, EN, SW Voltage 9V

VOUT Voltage.....6V

Operating Temperature Range .....–40°C to 85°C

Storage Temperature Range .....–55°C to 150°C

Thermal Resistance	Θ_{JA}	Θ_{JC}	
SOT23-5	220	110	°C/W

Lead Temperature (Soldering 10sec) .....260°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, unless otherwise specified. Typical values are at T_A = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.6		7	V
Input UVLO	Rising, Hysteresis=300mV		2.35	2.45	V
OVP	Rising, Hysteresis=400mV		7		V
Input Supply Current	V_{OUT}=1.2V, I_{OUT}=0A		6		mA
Input Shutdown Current				1	μA
Load Regulation	V_{OUT} =1.2V, I_{OUT} from 0.1A to 1A		0.1		%/A
Line Regulation	V_{IN}=2.7V to 5.0V and I_{OUT}=0.5A		0.1		%/V
Switching Frequency			3		MHz
PMOS Switch On Resistance	I_{SW}=200mA		200		mΩ
NMOS Switch On Resistance	I_{SW}=200mA		180		mΩ
High Side Current Limit		1.6			A
SW Leakage Current	V_{IN}=5.5V, V_{SW}=0 or 5.5V, EN= GND			5	μA
EN Logic High Threshold	Rising	1.2			V
EN Logic Low Threshold	Falling			0.4	V
EN Input Current	V_{EN}=5V		1	2	uA
Thermal Shutdown	Hysteresis=20°C		160		°C

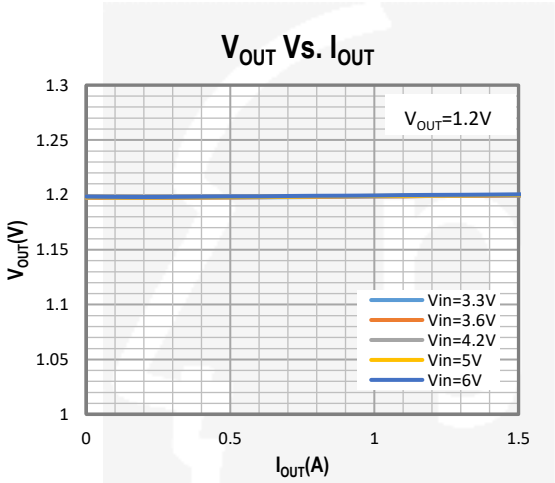
1.Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 2. Guaranteed by design, no production test

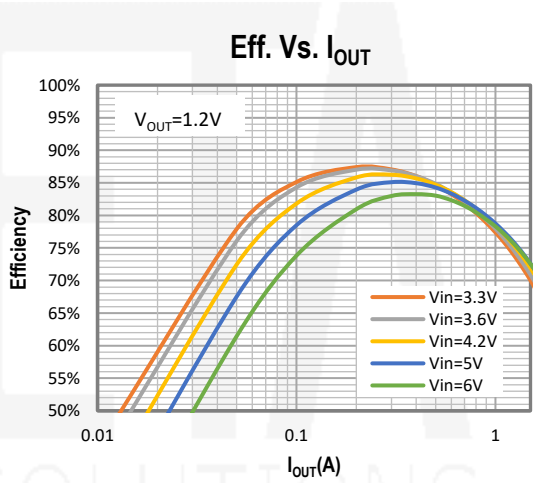
PIN DESCRIPTION

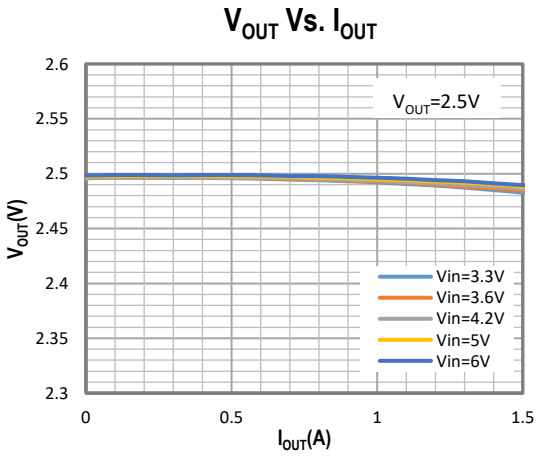
PIN #	NAME	DESCRIPTION
1	VIN	Supply voltage pin. Bypass with a 10μF ceramic capacitor to GND
2	GND	Ground
3	EN	Enable pin for the IC. Drive this pin high to enable the IC, low to disable. Default low when floating
4	VOUT	Output voltage pin. Bypass with a 10μF ceramic capacitor to GND
5	SW	Inductor connection. Connect an inductor between SW and the regulator output.

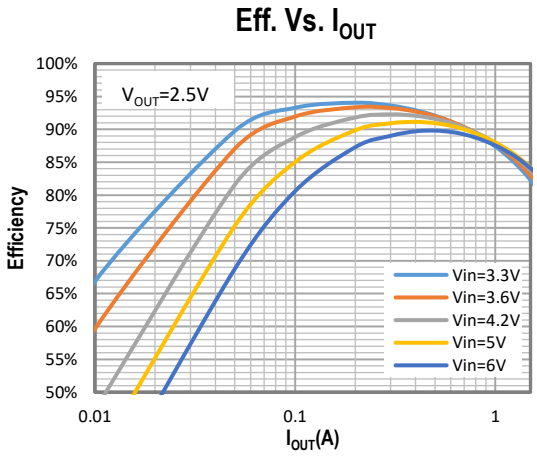
TYPICAL CHARACTERISTICS

(Typical values are at T_A = 25°C unless otherwise specified.)





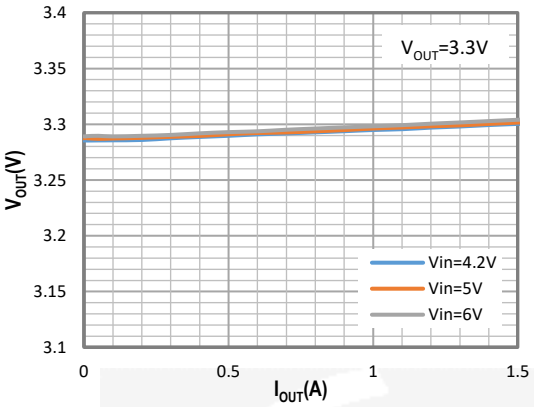




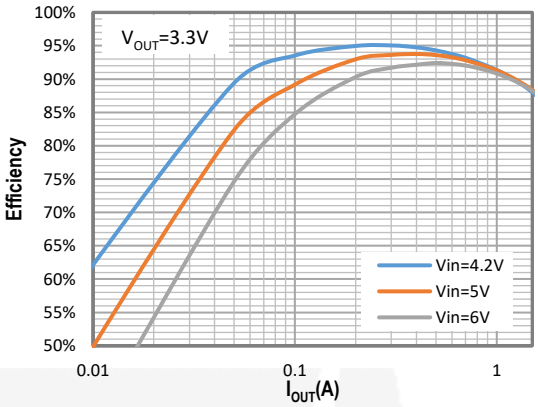
TYPICAL CHARACTERISTICS (cont')

(Typical values are at T_A = 25°C unless otherwise specified.)

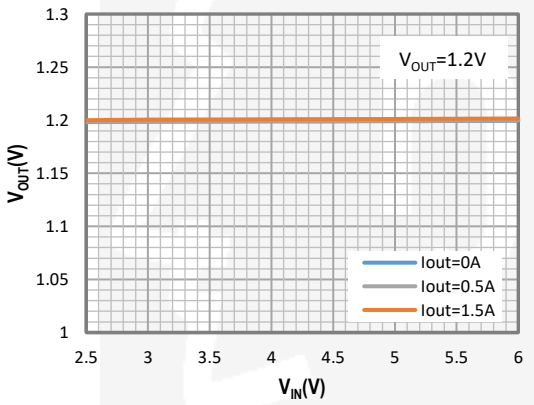
V_{OUT} Vs. I_{OUT}



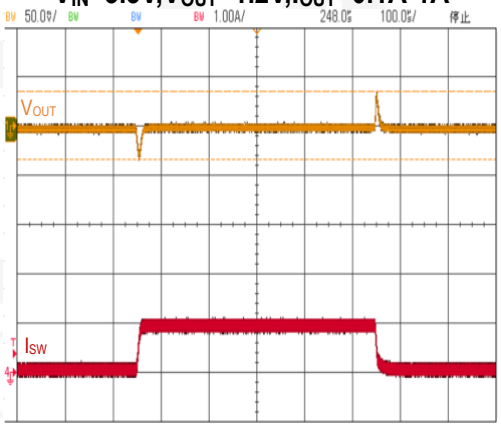
Eff. Vs. I_{OUT}



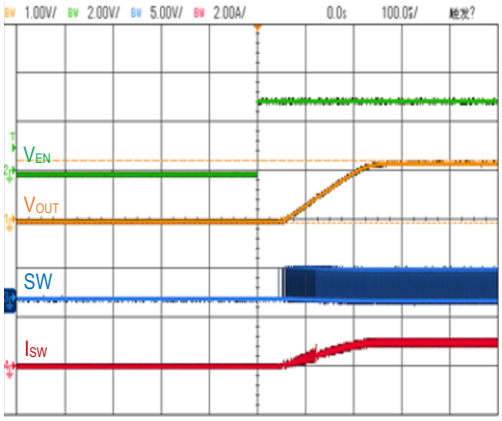
V_{OUT} Vs. V_{IN}



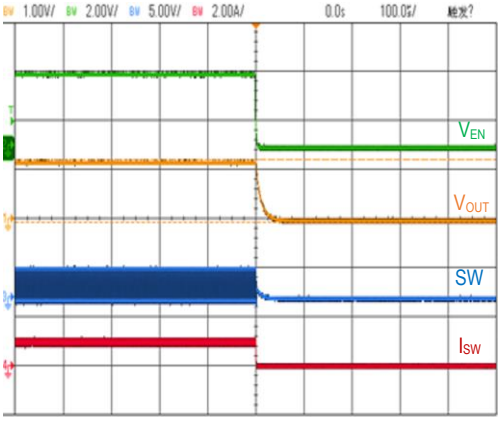
Load Transient
V_{IN}=3.3V,V_{OUT}=1.2V,I_{OUT}=0.1A-1A



Start Up from EN
V_{IN}=3.3V,V_{OUT}=1.2V,I_{OUT}=1A



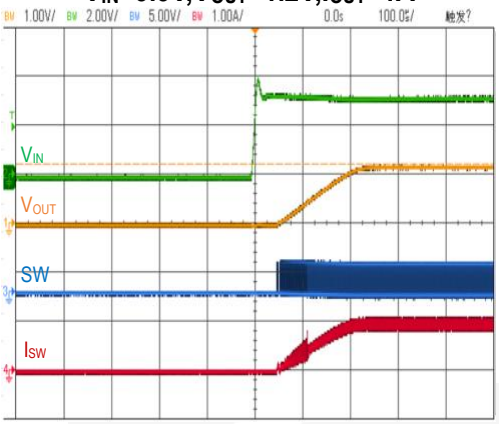
Shut Down from EN
V_{IN}=3.3V,V_{OUT}=1.2V,I_{OUT}=1A



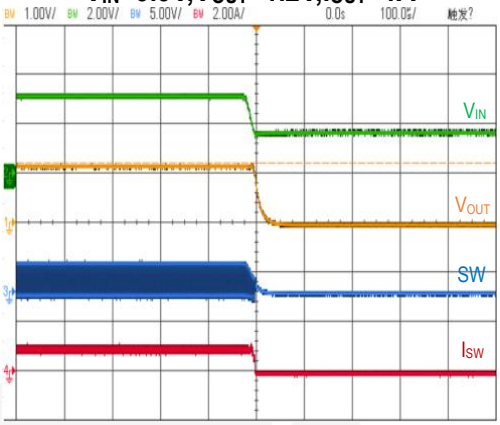
TYPICAL CHARACTERISTICS (cont')

(Typical values are at T_A = 25°C unless otherwise specified.)

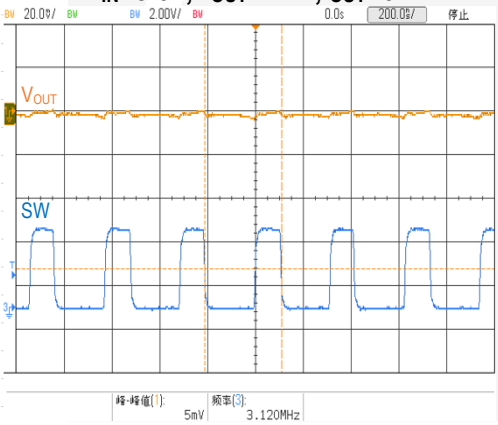
Start Up from VIN
V_{IN}=3.3V,V_{OUT}=1.2V,I_{OUT}=1A



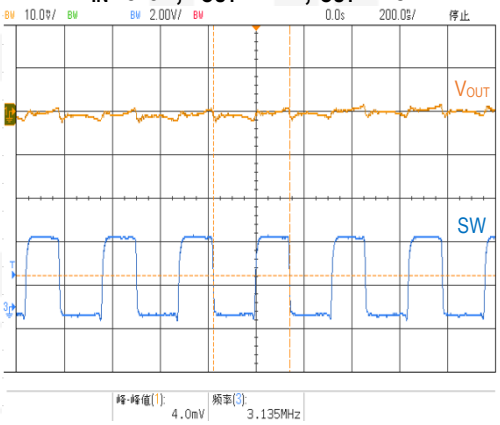
Shut Down from VIN
V_{IN}=3.3V,V_{OUT}=1.2V,I_{OUT}=1A



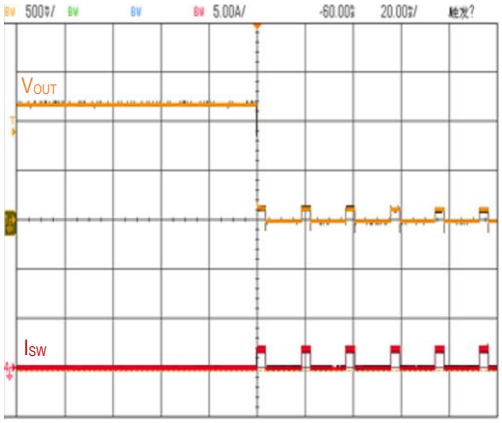
Output Voltage Ripple
V_{IN}=3.6V,V_{OUT}=1.2V,I_{OUT}=0A



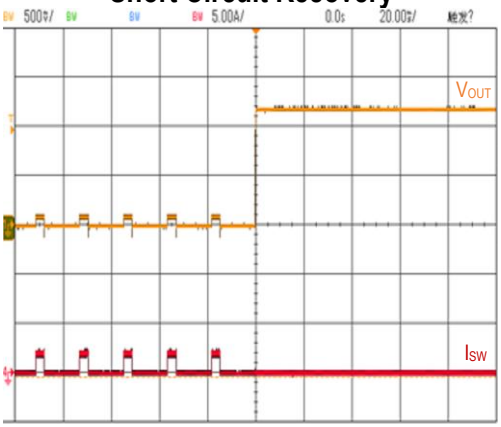
Output Voltage Ripple
**V_{IN}=3.6V,V_{OUT}=1.2V,I_{OUT}=1.5A



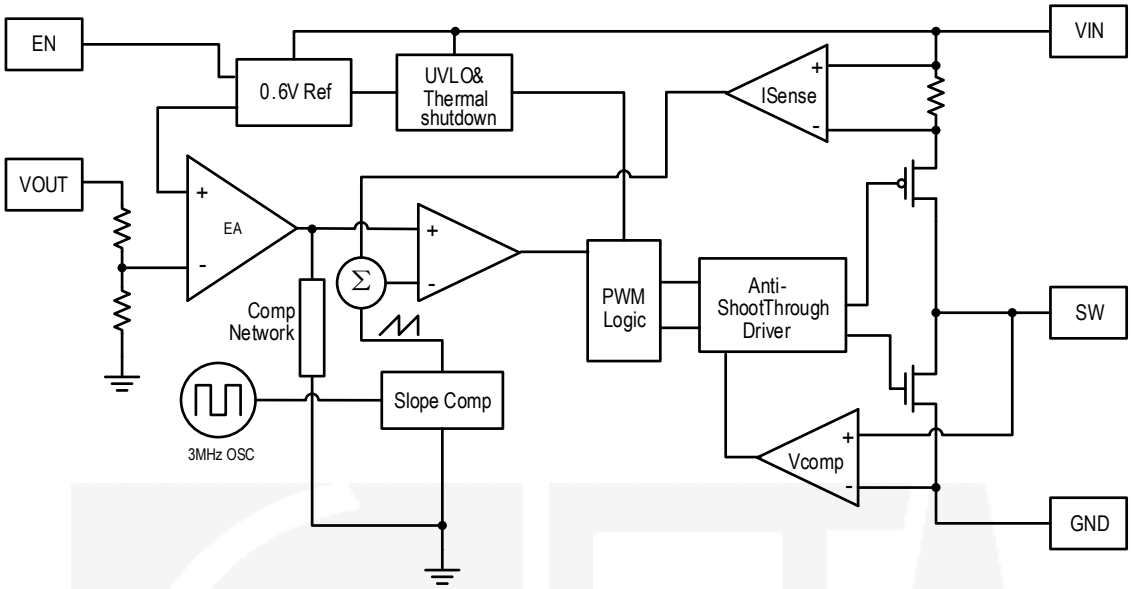
Short Circuit Protection



Short Circuit Recovery



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The ETA3424 high-efficiency switching regulator is a small, simple, DC-to-DC step-down converter, work in forced PWM mode, capable of delivering up to 1.5A of output current. The device operates in pulse-width modulation (PWM) at 3MHz with the input voltage from 2.6V to 7.0V and provides fixed output voltages of 1.2V, 2.5V and 3.3V, making the ETA3424 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

Loop Operation

ETA3424 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET. When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. ETA3424 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to I_{PEAK} and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

ETA3424 has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the I soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If IN drops below 2.05V, the UVLO circuit inhibits switching. Once IN rises above 2.35V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

DESIGN PROCEDURE

Input Capacitor and Output Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. Input ripple with a ceramic capacitor is approximately as follows:

$V_{RIPPLE} = IL_{(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{IN})]$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$V_{RIPPLE(ESR)} = IL_{(PEAK)} \times ESR$

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance.

Inductor Selection

A reasonable inductor value (LIDEAL) can be derived from the following:

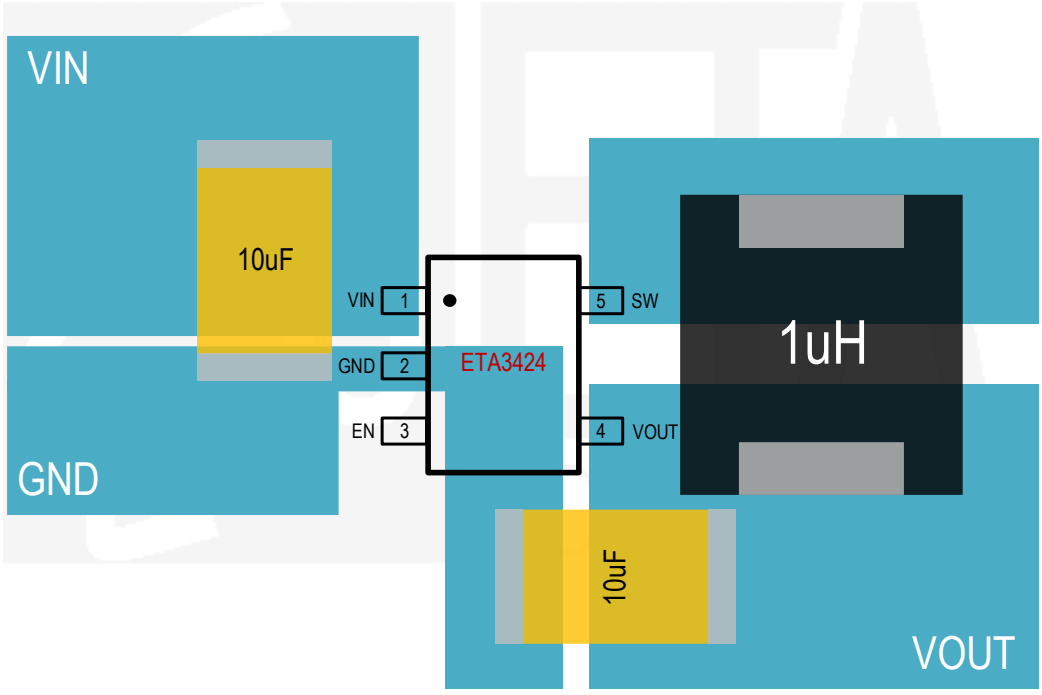
$L_{IDEAL} = [2(VIN) \times D(1 - D)] / I_{OUT} \times f_{OSC}$

PCB LAYOUT GUIDE

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

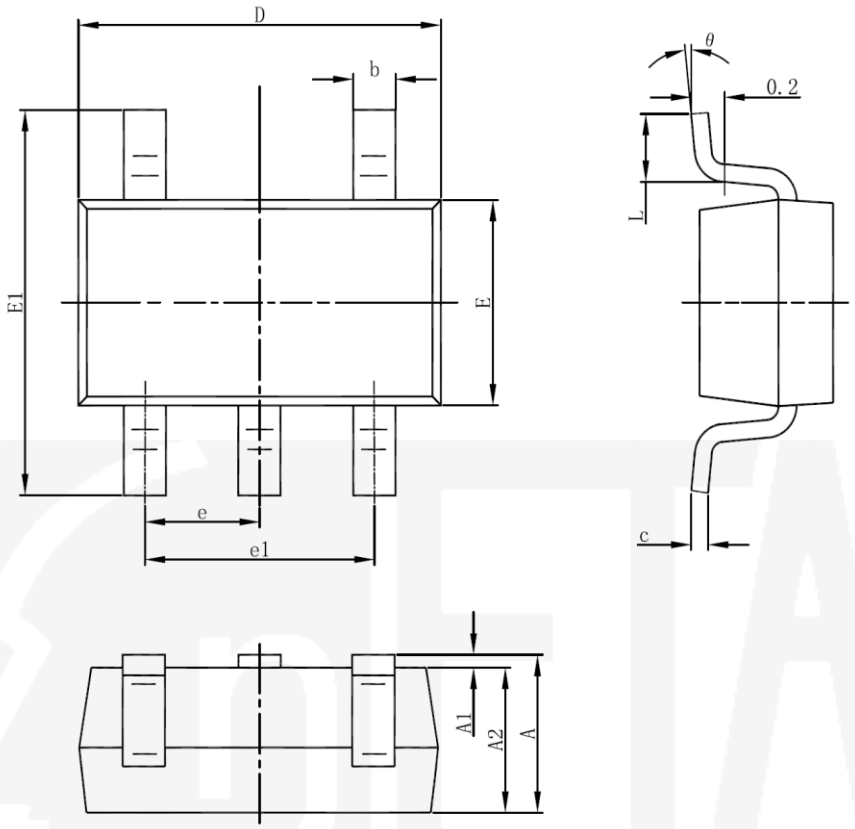
If change is necessary, please follow these guidelines and take Figure for reference.

1) Keep the path of switching current short and minimize the loop area formed by input cap, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the Vin pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Rout SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



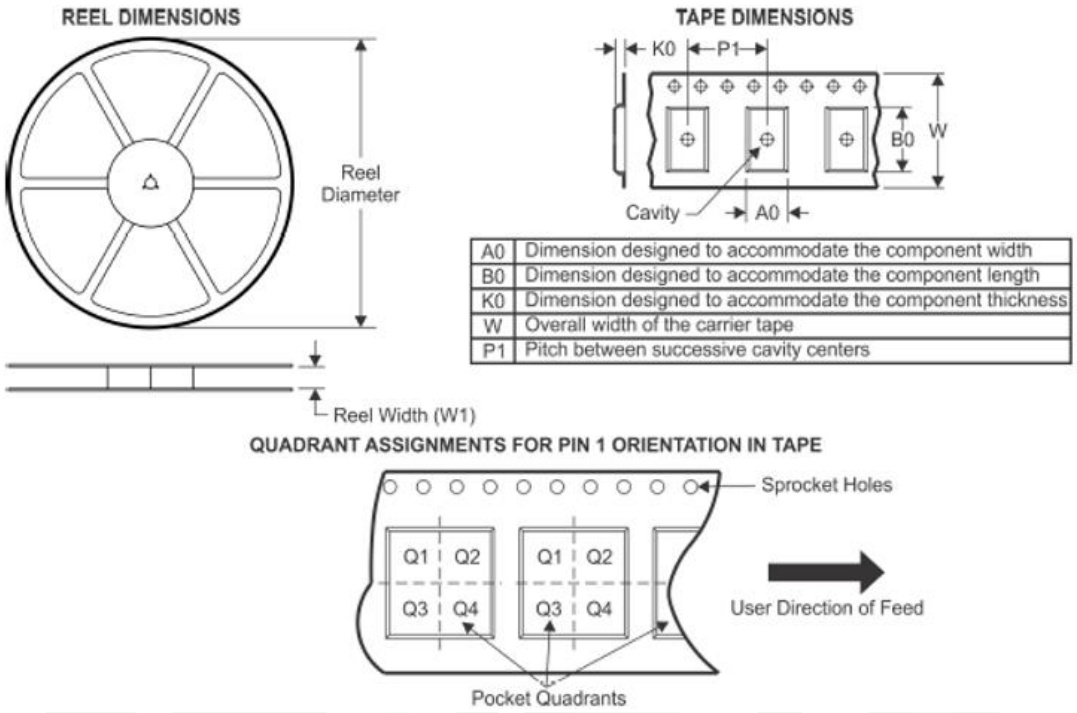
PACKAGE OUTLINE

Package: SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA3424VXXS2F	SOT23-5	5	3000	180	9.5	3.17	3.23	1.37	4	8	Q3