11A Input, 9V/3.5A Output Synchronous Boost with True-Shutoff

DESCRIPTION

The ETA1189 is a high-efficiency, synchronous boost from a wide range input voltage to a wide range programmable output voltage. With integrated high power MOSFETs, it can deliver up to 9V/3.5A output. It also has the true-shutoff function and real short circuit protection. These features with its tiny package of QFN3x3-20 make it an ideal all-in-one solution for high power boost applications.

The ETA1189 features a programmable output current limit, set by a resistor connected from ISET pin to GND. The output voltage can be also programmed by a resistor divider from VOUT to FB pin to GND. Besides external configuration, the ETA1189 features I²C communication which can be used to configure the current limit and output voltage internally. These features make it suitable for power delivery or quick charge applications.

The ETA1189 is available in a FCQFN3x3-20 package.

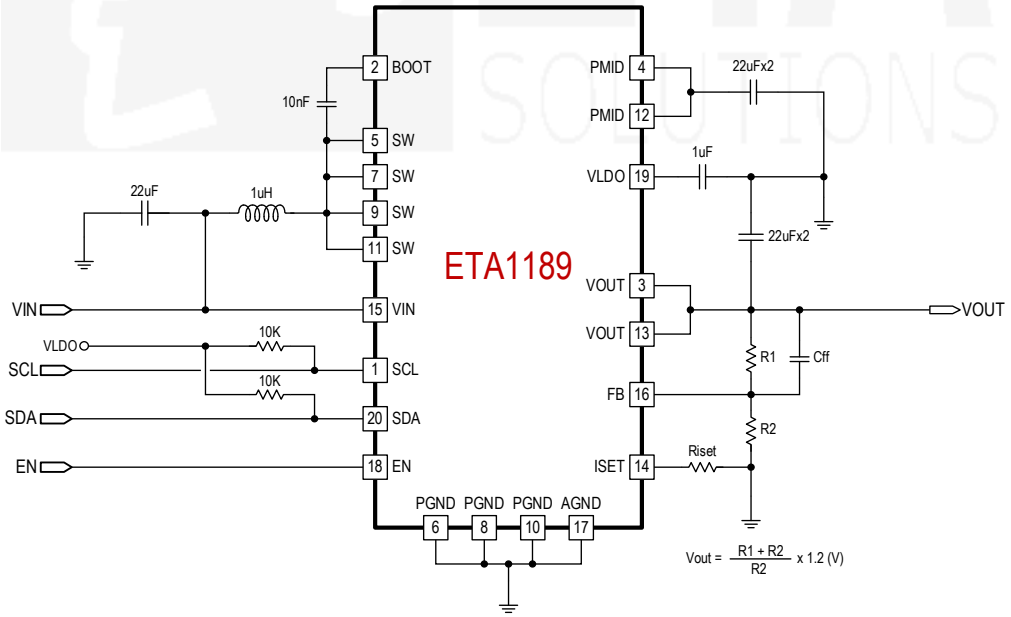
FEATURES

- Wide Input Voltage Range, 3.1V to 9.5V
- Wide Output Voltage Range, 3.6V to 12.6V
- True Shutoff with 20mΩ n-Chanel Pass Device
- Up to 95% High Efficiency
- High Efficiency at Light Load
- Programmable Current Limit, Output Voltage by External Resistor or Through I²C
- Accurate Output Current with CC Loop Regulation
- Up to 13A Cycle by Cycle Current Limit
- Small Footprint: FCQFN3x3-20 package
- RoHS Compliant

APPLICATIONS

- Quick Charge Mobile Power
- Bluetooth Speaker Supply
- Thunderbolt Interface
- Electronic Cigarette

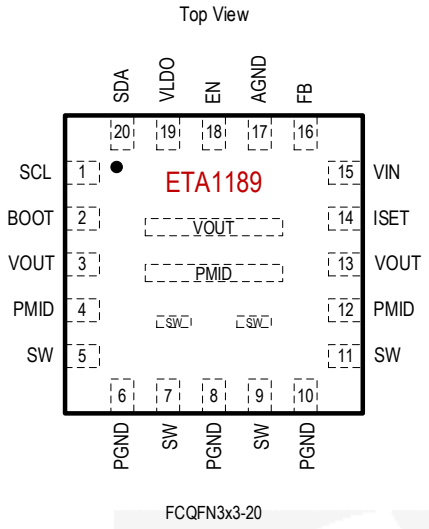
TYPICAL APPLICATION



ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA1189F3W	FCQFN3x3-20	ETA1189 YWW2L	5000

PIN CONFIGURATION



FCQFN3x3-20

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN Voltage to PGND.....–0.3V to 13.2V
VOUT, PMID, SW Voltage to PGND.....–0.3V to 16V
BOOT Voltage to SW.....–0.3V to SW+5V
All Other Pin Voltage to PGND.....–0.3V to 6V
SW,VIN,OUT to PGND current.....Internally limited
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C
Thermal Resistance θ_{JA}
FCQFN3X3-20.....30.....°C /W
Lead Temperature (Soldering, 10sec).....260°C

ELECTRICAL CHARACTERISTICS

(V_{IN} =3.3V, V_{OUT}=9V, AGND=PGND, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CONDITIONS						
VIN Input Voltage Range	VIN		3.1		9.5	V
Input Under-Voltage-Lock-Out	VIN_UVLO	VIN Rising		3.0		V
UVLO Hysteresis	VIN_UVLO_HYS	VIN Falling		0.2		V
Input Over-Voltage-Protection	VIN_OVP	VIN Rising		10		V
VIN_OVP Hysteresis	VIN_OVP_HYS	VIN Falling		0.5		V
Quiescent Current at PMID	IQ	EN=Logic High, No load, No Switching		200		μA
Shutdown Supply Current at VIN	ISD	EN=GND, V_{IN} = 4.2V		2	5	μA
Power Good Deglitch Delay	TPG	IN_UVLO < VIN < IN_OVP		1.5		ms
FREQUENCY CONFIGURATION						
Switching Frequency	FREQ	FREQUENCY[ ]=0, Default		500		KHz
		FREQUENCY[ ]=1		1000		KHz
OUTPUT CONFIGURATION						
Feedback Voltage	VFB	V_{OUT} =4.5V to 12.6V	1.176	1.2	1.224	V
FB Leakage Current	IFB			0		nA
ISET Pin Voltage	VISET	VOUT ≥ VOUT_LOWV	0.98	1.0	1.02	V
		VOUT < VOUT_LOWV	0.49	0.5	0.51	V

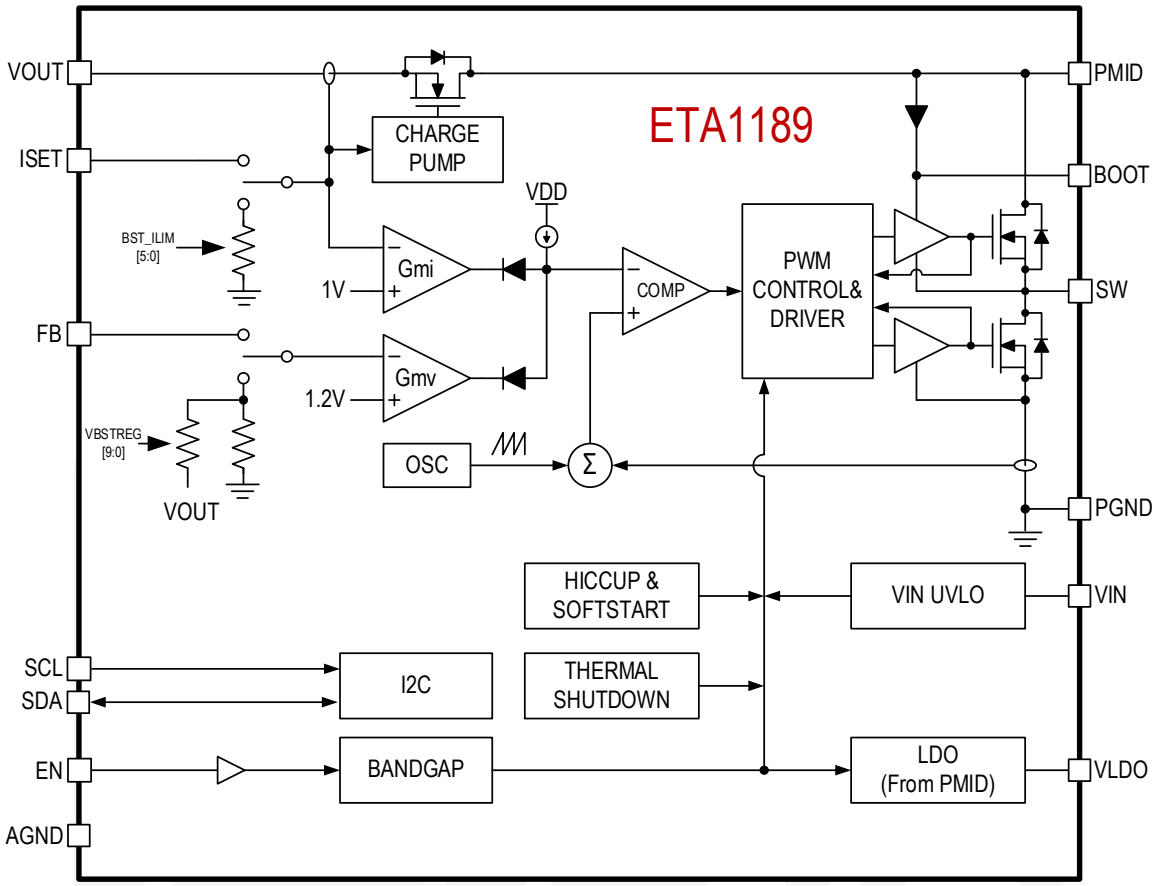
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ISET Output Current ratio	KISET	KISET = IQ1 / IISET		5000		
Output Current Limit	VOUT_ILIM	Adjustable, R_{ISET}=1.6KΩ		3.125		A
Output Current Foldback	VOUT_IFB	Adjustable, R_{ISET}=1.6KΩ		2		A
Switching Cycle-by-Cycle Low Side Current Limit	IPEAK			13		A
Minimum Inductor Current Each Cycle	IMIN			750		mA
Inductor Zero Crossing Current Stopping Threshold	IQZX			270		mA
PROTECTION						
VOUT Over Voltage Protection	VOUT_OVP			13.6		V
VOUT_OVP Hysteresis	VOUT_OVP_HYS			1		V
VOUT Enter Deep Condition Threshold	VDEEP_ENTER	VOUT Falling, VOUT-VIN		250		mV
VOUT Exit Deep Condition Threshold	VDEEP_EXIT	VOUT Rising over VIN		500		mV
Q1 Swapping Sensing Threshold	VOUT_LOWV	VOUT Rising		2.5		V
VOUT_LOWV Hysteresis	VOUT_LOWV _HYS	VOUT Falling		200		mV
FB Over-Voltage-Protection	VFB_OVP	To Stop Switching		1.38		V
VFB_OVP Hysteresis	VFB_OVP_HYS			60		mV
Output Under Voltage Protection	FB_UVP	Track FB pin Voltage		0.6		V
Hiccup Retrying Timer	THCON	Regulator Enabled		4.4		ms
Hiccup Disable Timer	THCOFF	Regulator Disabled		13.2		ms
Thermal Shutdown	TSD	Rising, Hysteresis=20°C		150		°C
LOGIC PINS, EN, SDA, SCL						
Input Current		2Meg Resistor from EN to GND, V_{EN} = 1V		1		μA
Logic High Voltage			1.2			V
Logic Low Voltage					0.4	V
POWER FETS						
PMID to OUT Switch On Resistance	RQ1			20		mΩ

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Side Switch On Resistance	RQ2			15		mΩ
Low Side Switch On Resistance	RQ3			12		mΩ
SW Leakage Current	SW_LKG	V_{OUT} = 9V, V_{FB}=1.5V, V_{SW}=0 or 9V, V_{EN}=GND			10	μA
INTERNAL VOUT SETTING						
VOUT Ramping Slew Rate	VOUT_SLEW	BST_SLEW[1:0] = 00		18		mV/μs
		BST_SLEW[1:0] = 01		9		
		BST_SLEW[1:0] = 10		4.5		
		BST_SLEW[1:0] = 11		2.25		
Internal VOUT Setting Range	VOUT_INT	Except the case of VBSTREG[9:0] = 1111111111	3.6		12	V
Internal VOUT Current Limit Range	ILIM_INT	EXT_ILIM[ ] = 0	450		3600	mA

PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	SCL	I²C interface clock. Connect a 10kΩ pull up resistor to VLDO or external 1.8V rail.
2	BOOT	Bootstrap capacitor connection for the high-side FET gate driver. Connect a 10nF ceramic capacitor (voltage rating ≥ 10V) from BOOT pin to SW pin.
3, 13	VOUT	Output pins. Connect a 2x22uF to GND
4, 12	PMID	Midpoint of the boost output and current limit switch. Connect a 2x22uF to GND
5, 7, 9, 11	SW	Switching pin. Connect with an inductor between this pin and input.
6, 8, 10	PGND	Power ground.
14	ISET	Boost maximum output current setting. Connect a resistor between this pin and analog ground to set the current level.
15	VIN	Input pin. Connect to the battery or input supply. Bypass with a 22uF capacitor from this pin to ground.
16	FB	Feadback pin for setting up the boost output voltage.
17	AGND	Analog ground pin.
18	EN	Enable pin for the IC.
19	VLDO	LDO regulator output. Bypass with 1uF capacitor from this pin to ground.
20	SDA	I²C interface data. Connect a 10kΩ pull up resistor to VLDO or external 1.8V rail.

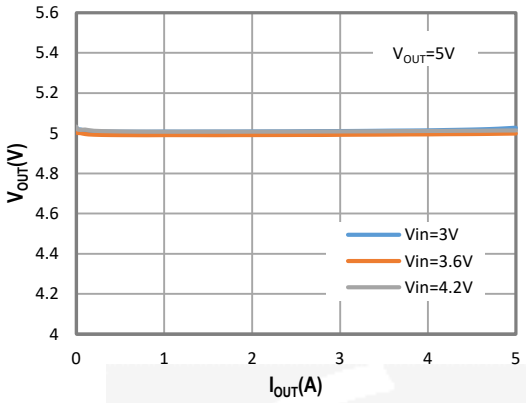
FUNCTIONAL BLOCK DIAGRAM



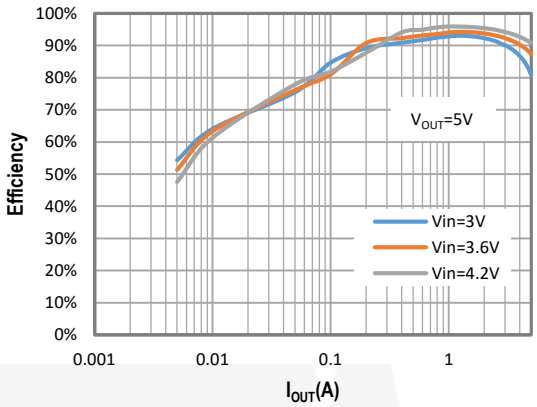
TYPICAL CHARACTERISTICS

(Typical values are at T_A = 25°C unless otherwise specified.)

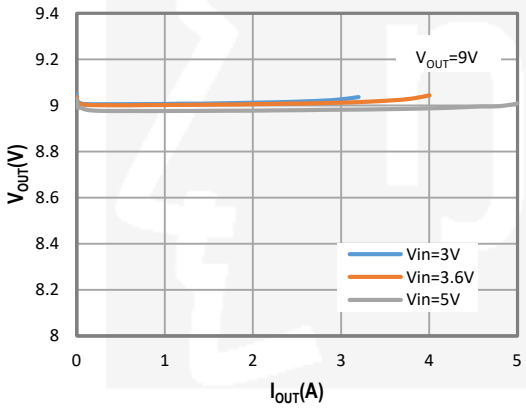
V_{OUT} Vs. I_{OUT}



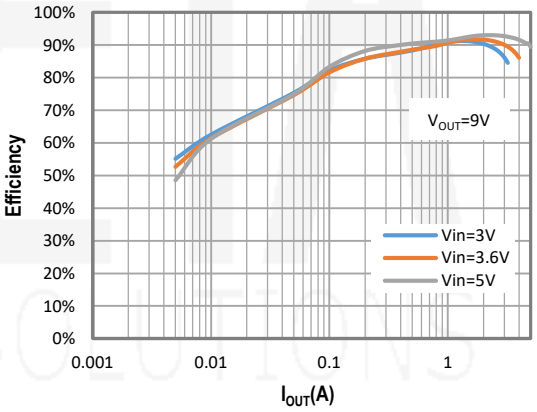
Eff. Vs. I_{OUT}



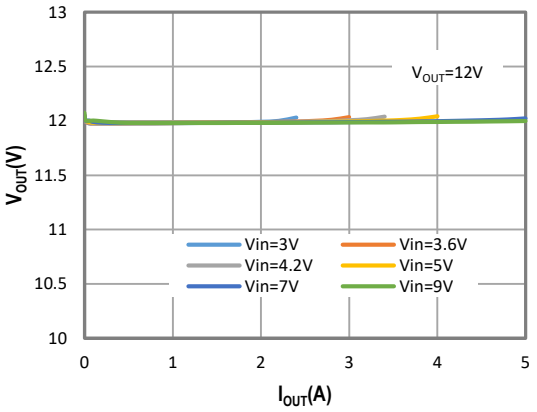
V_{OUT} Vs. I_{OUT}



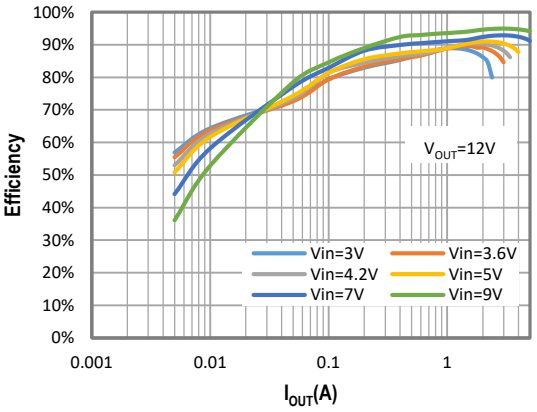
Eff. Vs. I_{OUT}



V_{OUT} Vs. I_{OUT}



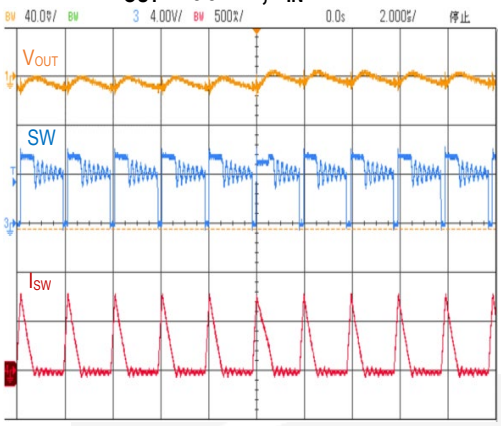
Eff. Vs. I_{OUT}



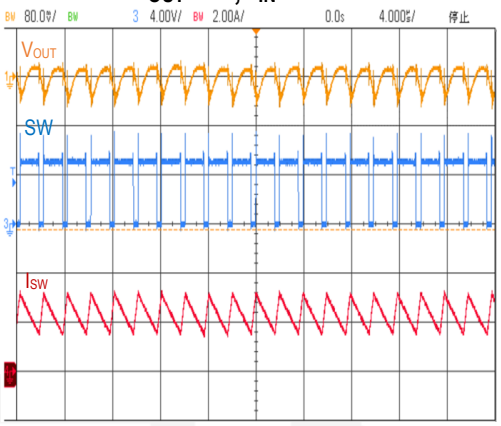
TYPICAL CHARACTERISTICS (cont')

(Typical values are at T_A = 25°C unless otherwise specified.)

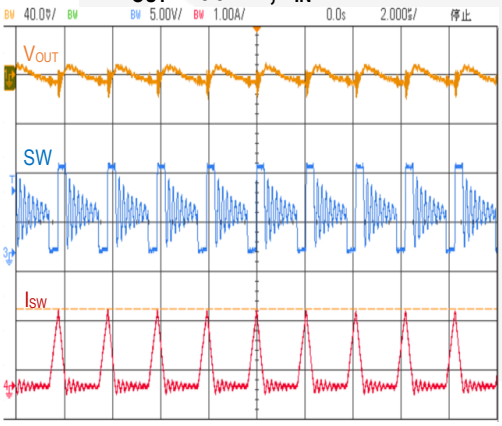
Switching in DCM, V_{OUT}=5V
I_{OUT}=100mA,V_{IN}=4.2V



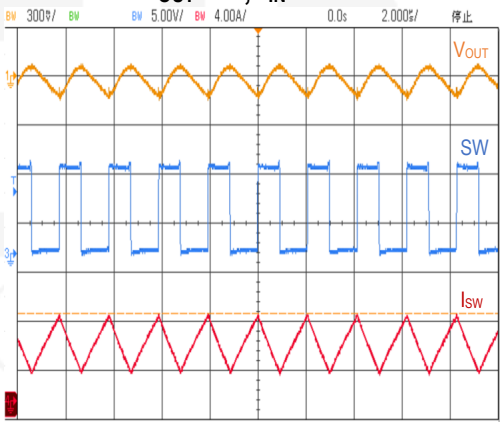
Switching in CCM, V_{OUT}=5V
I_{OUT}=2A,V_{IN}=4.2V



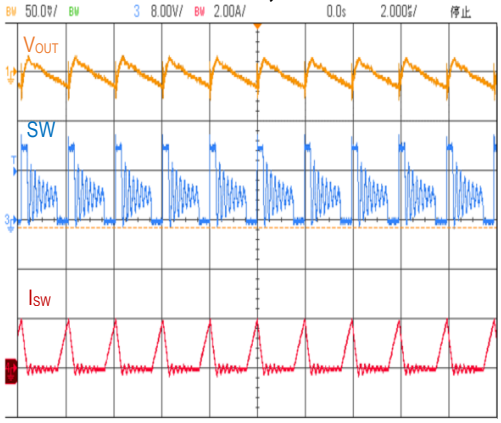
Switching in DCM, V_{OUT}=9V
I_{OUT}=100mA,V_{IN}=4.2V



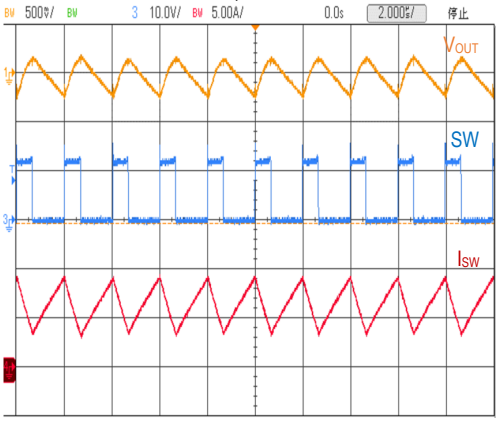
Switching in CCM, V_{OUT}=9V
I_{OUT}=2A,V_{IN}=4.2V



Switching in DCM, V_{OUT}=12V
I_{OUT}=100mA,V_{IN}=4.2V



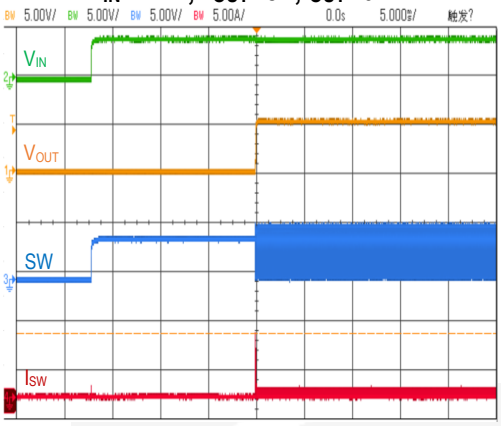
Switching in CCM, V_{OUT}=12V
I_{OUT}=2A,V_{IN}=4.2V



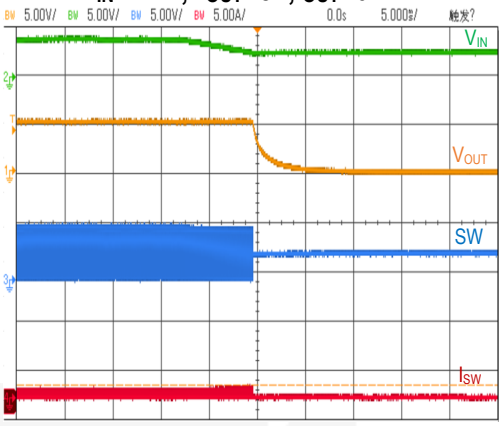
TYPICAL CHARACTERISTICS (cont')

(Typical values are at T_A = 25°C unless otherwise specified.)

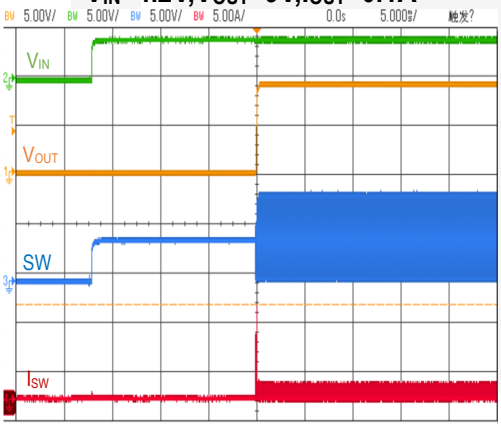
Start Up from VIN
V_{IN}=4.2V,V_{OUT}=5V,I_{OUT}=0.1A



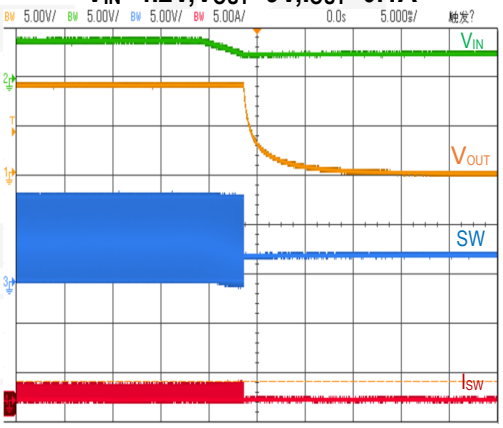
Shut Down from VIN
V_{IN}=4.2V,V_{OUT}=5V,I_{OUT}=0.1A



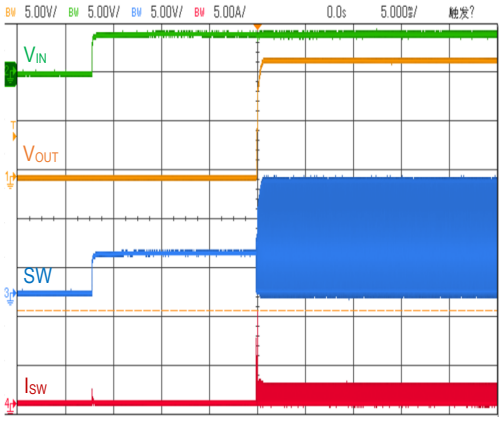
Start Up from VIN
V_{IN}=4.2V,V_{OUT}=9V,I_{OUT}=0.1A



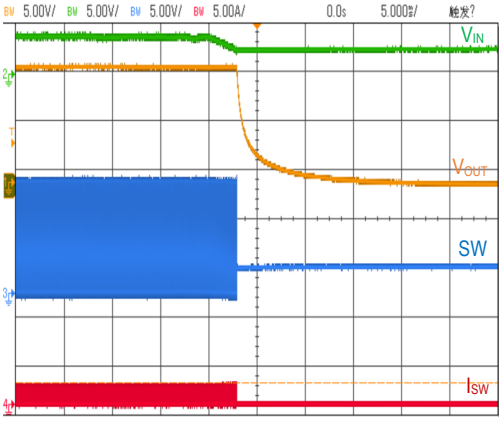
Shut Down from VIN
V_{IN}=4.2V,V_{OUT}=9V,I_{OUT}=0.1A



Start Up from VIN
V_{IN}=4.2V,V_{OUT}=12V,I_{OUT}=0.1A



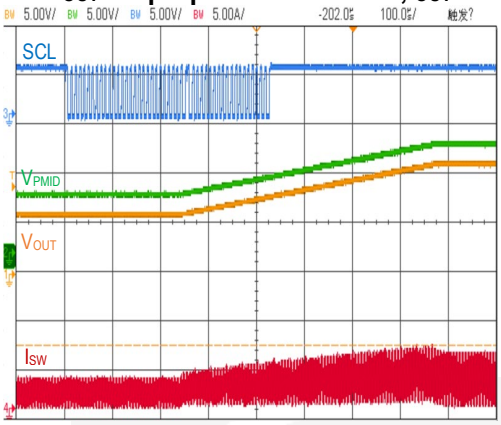
Shut Down from VIN
V_{IN}=4.2V,V_{OUT}=12V,I_{OUT}=0.1A



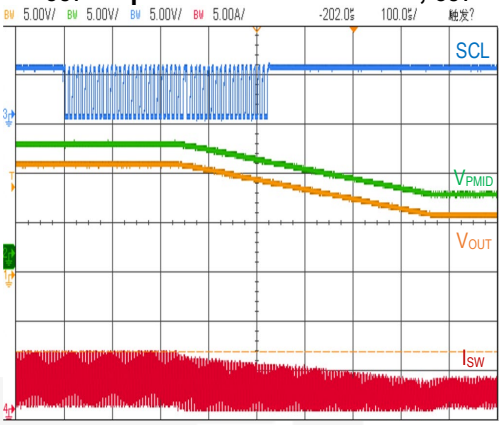
TYPICAL CHARACTERISTICS (cont')

(Typical values are at T_A = 25°C unless otherwise specified.)

I²C V_{OUT} Step Up 6.16V to 11.28V,I_{OUT}=1A



I²C V_{OUT} Step Down 11.28V to 6.16V,I_{OUT}=1A



FUNCTIONAL DESCRIPTION

START UP

ETA1189 is enabled when all following conditions occur:

- EN pin is asserted logic high
- VIN voltage is above VIN_UVLO
- VIN voltage is below VIN_OVP

Once enabling conditions are provided, a start-up is allowed to operate without VOUT_UVP and VOUT_OCP protections in 4ms before a HICCUP protection is enabled to protect part from output short.

Q1 will be enabled at the same time as the boost function. Q1 is controlled to operate differently in two modes, depending on the magnitude of the output VOUT versus the input VIN.

- VOUT is lower than VIN: Q1 FET operates with its current limit to limit VOUT output current at 80% of full VOUT current limit which is set by ISET resistor. In this mode, PMID is regulated to VIN+1V. The boost will stop switching if PMID voltage is above PMID_OVP level.
- VOUT is greater than VIN: Q1 FET gate will be drived to its maximum voltage. The boost will sense the current through Q1 and control the limit. Q1 FET will be disabled if VOUT is above VOUT_OVP level.

OUTPUT VOLTAGE REGULATION

An external feedback net is used to set the regulation level of the boost. FB pin is the input of the error amplifier which is regulated at 1.2V. Since Q1 is a separated path from PMID to Boost Output, Q1 can be disabled

separately with the boost. This makes Boost Output and PMID voltage may sometimes not be synchronous. So we choose PMID as regulation node, then feedback net is connected to PMID node to avoid PMID flying high in case Q1 is not in fully-on state.

The voltage regulation loop is compensated internally.

BOOST PFM/PWM OPERATION

ETA 1189 uses IMIN to determine PFM. The inductor current is required to be greater than IMIN each cycle. In the condition output current is small, load is below IMIN energy, it will make VOUT a little bit higher than regulation, ETA1189 will skip switching until VOUT fall below regulation level.

NEGATIVE INDUCTANCE PROTECTION

Besides PFM operation to improve efficiency when output current is low, ETA1189 also detects negative inductance current in discontinuous mode, then turns off high side FET Q2 judiciously. Finally, the efficiency is improved on whole discontinuous mode.

OUTPUT CURRENT LIMIT AND SWITCHING CURRENT PROTECTION

ETA1189 boost regulator is integrated with constant output current regulation that provides very accurate output current. Though, at low output condition output current limit is controlled by Q1 to avoid “boost current run away” condition. Anyway the switching inductor peak current is always limited at 13A (typically)

The output current is determined by the following rule:

VOUT CONDITION		Q1 BEHAVIOUR	BOOST CC REGULATION	ISET REGULATION VOLATGE
$V_{OUT} < V_{IN}+V_{DEEP}$	$V_{OUT} < V_{OLOWV}$			
NO	NO	Full Open	Activated	1V
YES	NO	Current Regulation	Inactivated	1V
ANY	YES	Current Regulation	Inactivated	0.5V

Output current level I_{BSTOUT} is set by the ISET pin resistor. The current of ISET pin is 1/5000 of Q1 current, then I_{BSTOUT} is given by the following equation:

$$I_{BSTOUT} = 5000 * \frac{V_{ISET}}{R_{ISET}(\Omega)}(A)$$

BOOST OUTPUT OVER VOLTAGE PROTECTION

At some conditions that VOUT could hit VOUT_OVP threshold, the boost will stop switching immediately and operate again when VOUT goes back to normal. In this condition, Q1 is still fully turned on.

Besides PMID over voltage protection, ETA1189 integrates FB over voltage protection that when FB voltage hits VFB_OVP, the boost will stop switching immediately and operate again when FB goes back to normal. This feature can protect output-connected device when VIN is higher than the regulation level.

BOOST HICCUP OPERATION

During operation if one of VOUT_UVP or VOUT_OCP occurs, ETA1189 starts HICCUP mode that both Q1 and boost are disabled in 12ms then retried in 4ms. It will exit HICCUP mode when fault conditions are removed in 4ms retrying.

THERMAL SHUTDOWN

ETA1189 is shutdown when the junction temperature gets higher than 150˚C. And it will be back to normal operation when it is cooler than 130˚C.

APPLICATION INFORMATION

OUTPUT VOLTAGE CONFIGURATION

The FB pin voltage is regulated to 1.2V, so feedback resistors are given by the following equation:

$$V_{OUT} = 1.2 * \frac{R_1 + R_2}{R_2} \quad (V)$$

For example, when R_2 = 55KΩ, R_1 is given by the below table:

V_{OUT}(V)	R_1(KΩ)	V_{OUT}(V)	R_1(KΩ)
5.06	180	9.13	370
5.91	220	10.41	430
6.99	270	11.27	470
8.27	330	12.13	510

OUTPUT CURRENT LIMIT CONFIGURATION

$$I_{BSTOUT} = 5000 * \frac{V_{ISET}}{R_{ISET}(\Omega)} (A)$$

INTERNAL SETTING BY I²C

Besides the external configuration for VOUT and ILIM, ETA1189 also provides an I²C protocol to set VOUT and ILIM internally. Once VBSTREG[9:0] is not all 1, there is an internal feedback net which is started to set VOUT from 3.6V to 12.08V.

$$V_{BSTOUT} = 3.6V + 0.01V * \sum_{i=0}^{9} \{2^i * VBSTREG[i]\}$$

And ILIM can be set from 450mA to 3600mA.

$$\mathrm{ILIM} = 450\mathrm{mA} + 50\mathrm{mA} * \sum_{i=0}^{5} \{2^i * \mathrm{BST\_ILIM}[i]\}$$

REGISTER MAP

		00	REG01: STATUS REGISTER	
7	OTG_STAT[1:0]	0	Read Only	Boost Regulation Status: => 00: Not Boosting => 01: In CC Regulation => 10: In CV Regulation => 11: Hiccup Protection
6		0	Read Only	
5	RFU	0	Read Only	Reverse for Future Use
4	BAT_DEEP_FAULT	0	Read Only	Battery is over discharged in Boost Mode status: => 0: Battery is not discharged to below UVLO => 1: Battery is discharged to below UVLO
3	PMID_OVP_FAULT	0	Read Only	Boost Output Over Regulation Status: => 0: VPMID is below 110% of Regulation => 1: VPMID is above 110% of Regulation
2	BST_ILIM_FAULT	0	Read Only	Boost Inductor Switching status: => 0: Inductor current not hit I_LIM_BST => 1: Inductor current hits I_LIM_BST
1	VPMID_PG	0	Read Only	Boost Output Power Good Status: => 0: VPMID is below 90% of Regulation => 1: VPMID is above 90% of Regulation
0	OTGIN_PG	0	Read Only	Boost Input Supply Status: => 0: VBATS is below VBST_UVLO or above VBST_OV => 1: VBST_UVLO < VBATS <VBST_OV
		FF	REG05: BOOST OUTPUT CONFIGURATION REGISTER	
7	VBSTREG[7:0]	1	RD/WR	Internal VBUS Regulation: => LSB = 10mV, MSB = 5120mV => Offset = 3.6V (Defined as minimum of setting) => Limit at 12.08V =>VBSTREG[9:0] = 1111111111 to use external setting (Default)
6		1	RD/WR	
5		1	RD/WR	
4		1	RD/WR	
3		1	RD/WR	
2		1	RD/WR	
1		1	RD/WR	
0		1	RD/WR	
		03	REG06: BOOST OUTPUT CONFIGURATION REGISTER	
7	RFU	0	RD/WR	Reverse for Future Use
6		0	RD/WR	
5		0	RD/WR	
4		0	RD/WR	
3	RFU	0	RD/WR	Reverse for Future Use
2		0	RD/WR	
1	VBSTREG[9:8]	1	RD/WR	Internal VBUS Regulation => VBSTREG[8] = 2560mV => VBSTREG[9] = 5120mV
0		1	RD/WR	

		7F	**REG07: Q1 LIMIT CONFIGURATION REGISTER**	
7	BST_ILIM [5:0]	0	RD/WR	Internal VBUS Current Limit Configuration: => LSB = 50mA, MSB = 1600mA => Offset = 450mA (Defined as minimum of setting) => BST_ILIM[5:0] = 011111 for 2A as Default
6		1	RD/WR	
5		1	RD/WR	
4		1	RD/WR	
3		1	RD/WR	
2		1	RD/WR	
1	EN_BSTILIM	1	RD/WR	Enable boost CC current limit. => 1 (default): Follow table setting, default 2A. => 0: Boost CC=5A. (It just like a protection function only.)
0	EXT_ILIM	1	RD/WR	Switch between External CC ILIM and internal CC ILIM => 1 (default): external ILIM (follow RISET) => 0: Internal ILIM (follow setting table)
		16	**REG08: CONTROLLER REGISTER**	
7	RESET	0	RD/WR	Register Reset: => Write 1 to reset the register and regulator. Auto clear to 0 after chip is reset
6	HIZ_MODE	0	RD/WR	High Impedance Mode: => 0: Normal Operation (Default) => 1: Force Part in HIZ mode
5	WD_TIMER	0	RD/WR	Watchdog Timer Setting: => 0: Disable Timer (Default) => 1: 40s to reset all register
4	OTG_MODE	1	RD/WR	OTG Mode: => 0: Disable Boost => 1: Enable Boost (Default)
3	WD_RESET	0	RD/WR	Watchdog Timer Reset: => Write 1 to reset Watchdog Timer => Reed 1 means watchdog timer expired
2	Q1_ENABLE	1	RD/WR	Q1 Enable in Boost Mode. Set to 0 for power bank application => 0: Disable Q1 => 1: Enable Q1 (Default)
1	Q1_FULLON	1	RD/WR	Q1 FET scaled by current limit: => 0: Scale for better sensing => 1: Force full on (Default)
0	FREQUENCY	0	RD/WR	Switching Frequency => 0: 500kHz (Default) => 1: 1000kHz (Less Output Capacitor Care)
		00	**REG09: OUTPUT CORD COMPENSATION CONFIGURATION REGISTER**	
7	BST_CORD[3:0]	0	RD/WR	

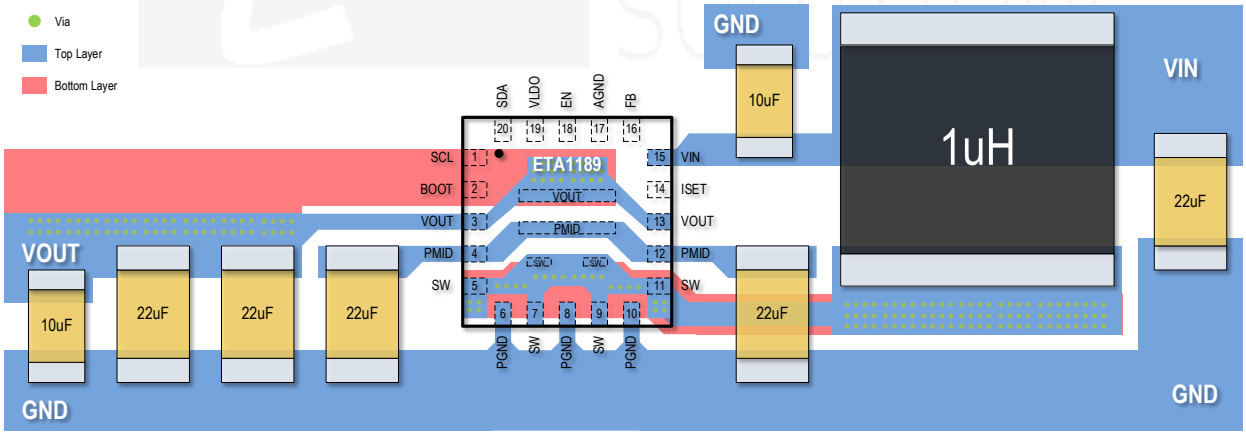
6		0	RD/WR	Boost Regulation Cord Compensation Setting:
5		0	RD/WR	=> LSB = 20mΩ
4		0	RD/WR	=> MSB = 160mΩ
				=> Default is no compensation
3	BST_SLEW[1:0]	0	RD/WR	Dynamic voltage scale slew rate change for internal FB
2		0	RD/WR	(default 00)
				=> 00: 18mV/μs => 01: 9mV/μs
				=> 10: 4.5mV/μs => 11: 2.25mV/μs
1	RFU	0	RD/WR	Reverse for Future Use
0	RFU	0	RD/WR	Reverse for Future Use

PCB LAYOUT GUIDE

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

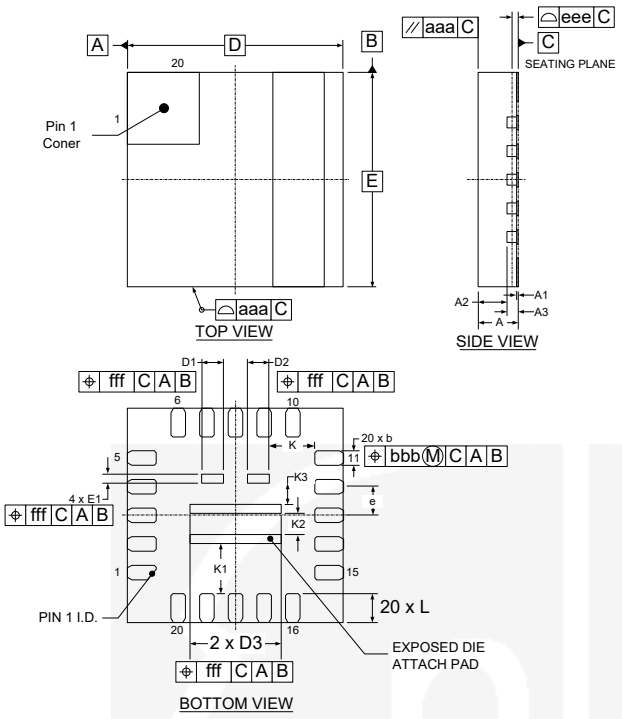
If change is necessary, please follow these guidelines and take Figure for reference.

1) Keep the path of switching current short and minimize the loop area formed by input cap, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the Vin pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Rout SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



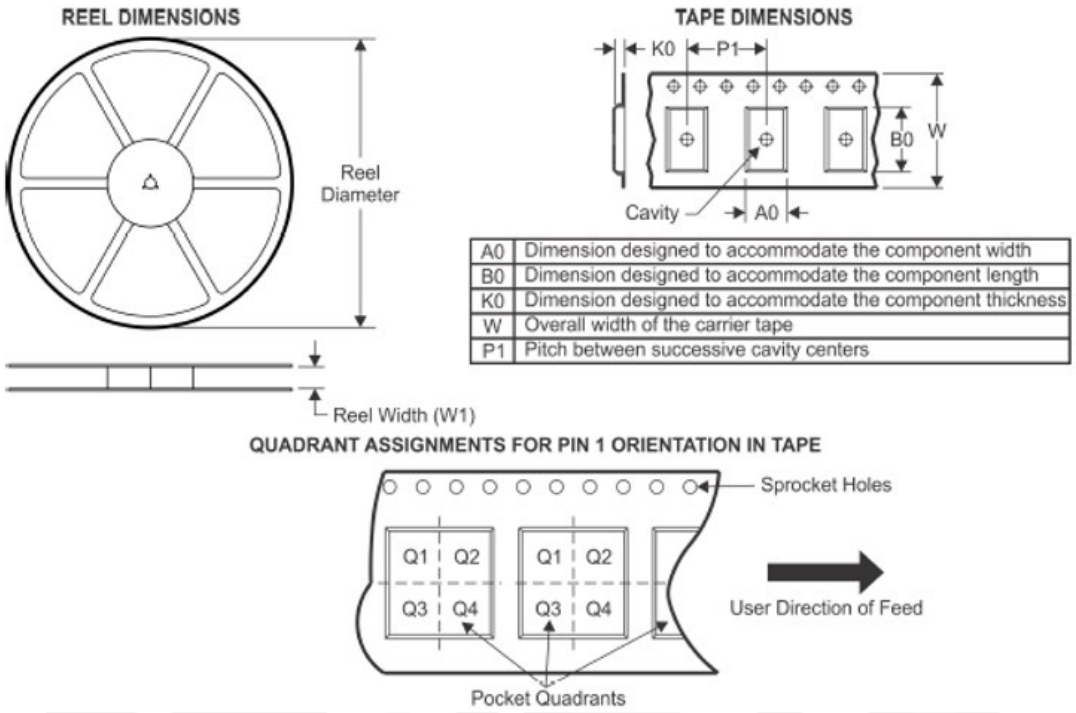
PACKAGE OUTLINE

Package: FCQFN3x3-20



		SYMBOL	MIN	TYP	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3	0.152 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	3 BSC		
	Y	E	3 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D1	0.2	0.3	0.4
		D2	0.2	0.3	0.4
		D3	1.17	1.27	1.37
	Y	E1	0.02	0.12	0.22
LEAD LENGTH		L1	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K	0.63 REF		
		K1	0.71 REF		
EXPOSED PAD TO EXPOSED PAD EDGE		K2	0.3 REF		
		K3	0.3 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA1189F3W	FCQFN3x3-20	20	5000	330	12.4	3.35	3.35	1.13	8	12	Q1