ETA1168

40V Step-Up Regulator for White LED Driver with PWM Dimming

DESCRIPTION

The ETA1168 is a high efficiency step-up converter with an internally integrated 40V power MOSEFT. It runs with an optimal 600KHz frequency that enables the use of small external components while still providing the best efficiency. It can drive up to 10 to 12 LEDs in series and also in parallel combinations. The incorporated true PWM-Diming feature through CTRL pin does not generate audible noise on the output capacitor during diming because it does not burst the LED current. For maximum protection, the ETA1168 has an OVP protection feature that prevents the output voltage exceeding the maximum rating of the ETA1168 and the output cap during open-LED conditions.

ETA1168 is available in a space-saving DFN22-6 package.

FEATURES

- **Up to 92% Efficiency**
- **40V OVP protection**
- **True PWM Brightness Control**
- **200mV Feedback Voltage**
- DFN2x2-6 Package

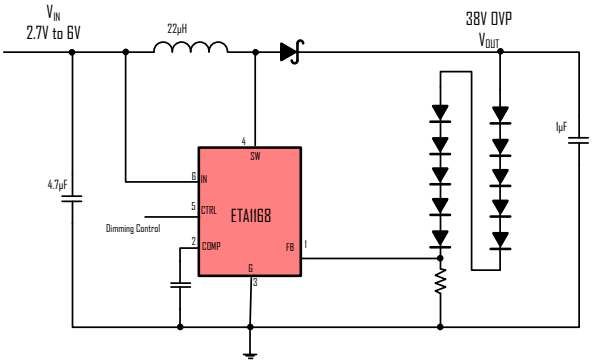
APPLICATIONS

- LED Backlighting for Tablets, MIDs and Smartphones
- LED Driver

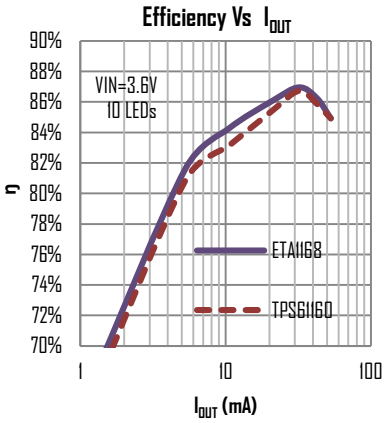
ORDERING INFORMATION

PART #	PACKAGE PIN	TOP MARK
ETA1168D2G	DFN2x2-6	DGYW Date Code Product Number

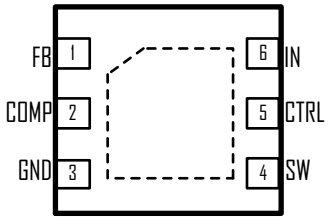
TYPICAL APPLICATION



Same Board, same everything else, ETA1168 beats TI's TPS61160 in Efficiency handily across the board



PIN CONFIGURATION



DFN2x2-6

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

SW Voltage.....-0.3V to 40V
All Other PIN Voltages.....-0.3V to 6.5V
SW to ground current .....Internally limited
Operating Temperature Range .....-40°C to 85°C
Storage Temperature Range .....-55°C to 150°C

Thermal Resistance	θ_{JA}	θ_{JC}	
DFN2x2-6	80	30	°C/W

ELECTRICAL CHACRACTERISTICS

(V_{IN} = 3.6V, unless otherwise specified. Typical values are at TA = 25°C.)

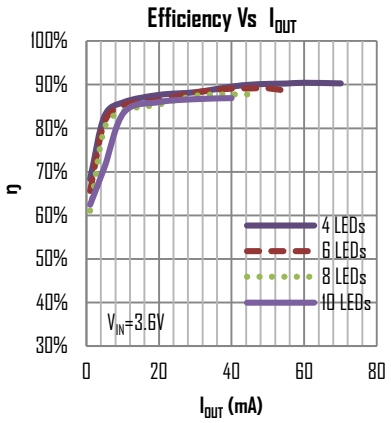
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.7		6	V
FB Feedback Voltage	V_{IN} = V_{CTRL} =3.6V	194	200	206	mV
FB Input Current				50	nA
Quiescent Current at IN	Switching			1.8	mA
	No Switching		0.6		mA
Shutdown Supply Current at IN	V_{EN}=GND		0	5	μA
Switching Frequency	V_{IN}<4.3V		600		KHz
Maximum Duty Cycle		90			%
NMOS Switch On Resistance	I_{SW} =100mA		0.3		Ω
NMOS Switch Current Limit			700		mA
SW Leakage Current	V_{SW}=0 or 38V, V_{EN}=GND			10	μA
COMP GM			300		μmho
CTRL Input Current			0.1	1	μA
CTRL Input Low Voltage				0.6	V
CTRL Input High Voltage		1.2			V
Thermal Shutdown	Rising, Hysteresis=10°C		165		°C

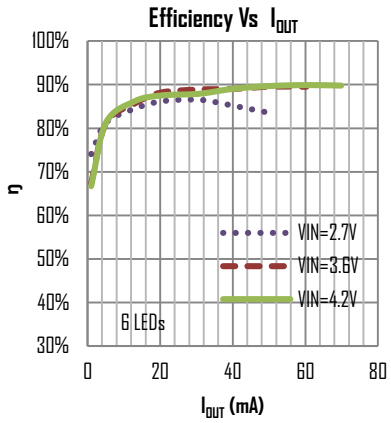
PIN DESCRIPTION

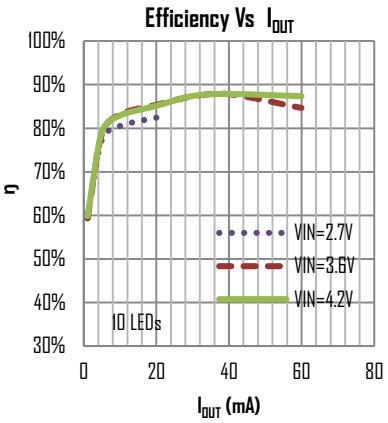
PIN #	NAME	DESCRIPTION
1	FB	Feedback Input for Current. Connect an external resistor FB to GND to set I_{OUT}
2	COMP	External Compensation Pin. Connect an capacitor from this pin to GND to compensate
3	GND	Ground Pin
4	SW	Inductor Connection. Connect an inductor Between SW and IN.
5	CTRL	Control pin for the IC. It is a multi-functional pin for enable control, PWM dimming
6	IN	Input Supply pin. Bypass with a 4.7μF or larger ceramic capacitor to GND

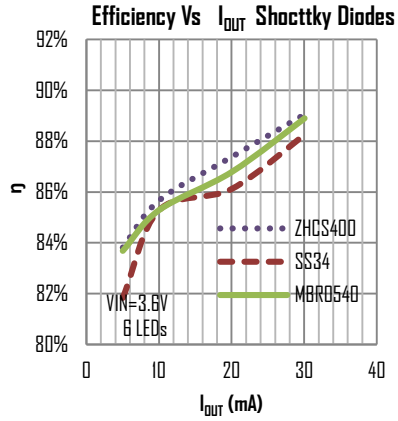
TYPICAL CHARACTERISTICS

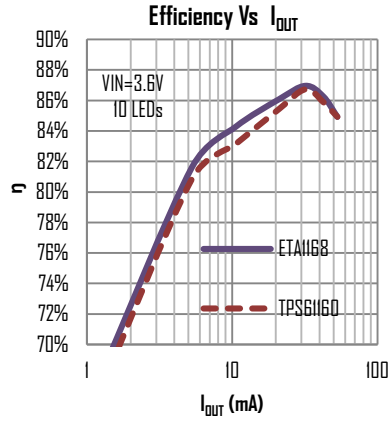
(Typical values are at TA = 25°C unless otherwise specified.)

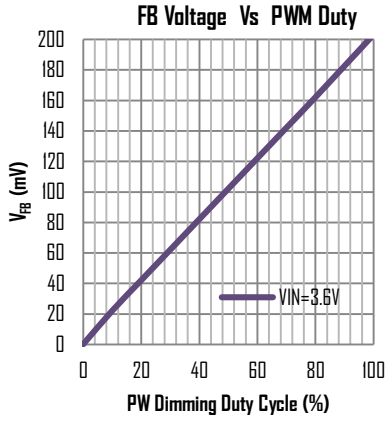




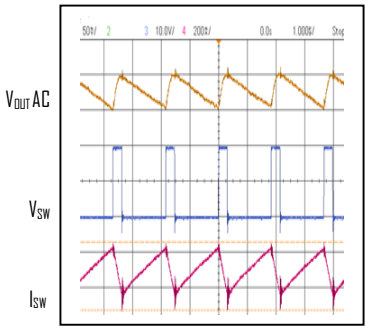






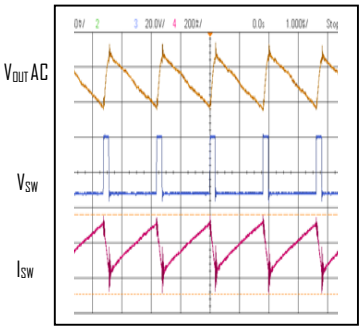


Switching Waveform
VIN=3.6V, 6 LEDs, IOUT= 20mA



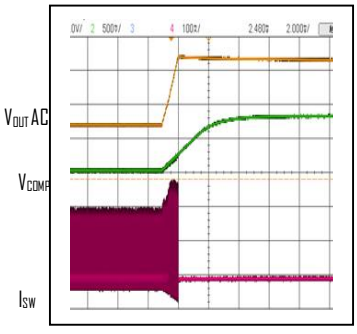
1μs/div

Switching Waveform
VIN=3.6V, 10 LEDs, IOUT= 20mA



1μs/div

Over Voltage Protection



2ms/div

FUNCTIONAL DECRIPTIONS

The ETA1168 is a high efficiency, high output voltage boost converter in a small package size. The device is ideal for driving white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40V/0.7A switch FET and operates in pulse width modulation (PWM) with 600kHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The feedback loop regulates the FB pin to a low reference voltage (200mV typical), reducing the power dissipation in the current sense resistor.

Open LED Protection

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The ETA1168 monitors the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the IC when both of the following conditions persist for 8 switching clock cycles: (1) the SW voltage exceeds the VOVP threshold and (2) the FB voltage is less than half of regulation voltage. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin logic. The maximum forward voltage plus the 200mV reference voltage cannot exceed the minimum OVP threshold or (nLEDS X VLED(MAX)) + 200 mV ≤ VOVP(MIN).

Shutdown

The ETA1168 enters shutdown mode when the CTRL voltage is logic low for more than 2.5ms. During shutdown, the input supply current for the device is less than 1μA (max). Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. However, in the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the Schottky and keep leakage current low.

Current Programming

The FB voltage is regulated by a low 0.2V reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the RSET is calculated using Equation 1:

ILED =VFB/RSET (1)

Where

ILED = output current of LEDs,VFB = regulated voltage of FB,RSET = current sense resistor

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

PWM Dimming Control

When the CTRL pin is constantly high, the FB voltage is regulated to 200mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 2.

VFB =Duty*200 mV (2)

Where

Duty = duty cycle of the PWM signal, 200 mV = internal reference voltage

This PWM dimming eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, ETA1168 regulation voltage is independent of the PWM logic voltage level which often has large variations For optimum performance, use the PWM dimming frequency in the range of 5kHz to 100kHz.

APPLICATION INFORMATION

Inductor Selection

Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10μH to 22μH inductor value range is recommended. A 22μH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple. Below table lists the recommended inductor for the ETA1168.

Recommended Inductors for ETA1168

Part #	L(μH)	Saturation Curent (mA)	Vendor
SWRH3D16S	10-22	>750	Sunlord

Schottky Diode Selection

A high-speed rectifying Schottky is recommended for ETA1168 for maximum efficiency due to its high switching frequency. The diode average and peak current rating must be larger than the average output current and peak inductor current to ensure reliability. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. The ONSemi MBR0540 and the ZETEX ZHCS400 are recommended for ETA1168. A typically efficiency performance comparison for these diodes is also shown in the TYPICAL CHARACTERZATION section.

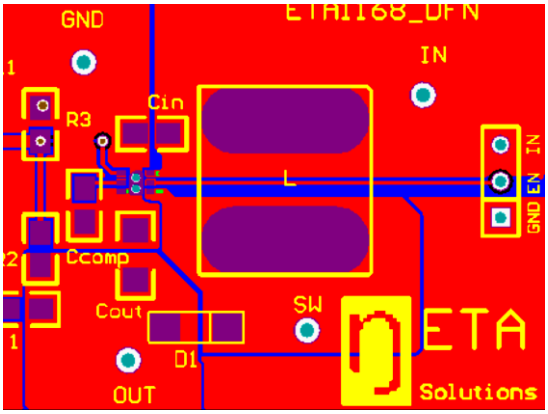
Compensation Capacitor Selection

The compensation capacitor, connected from COMP pin to GND is used to stabilize the feedback loop of the ETA1168. A 220nF ceramic compensation capacitor is suitable for most applications.

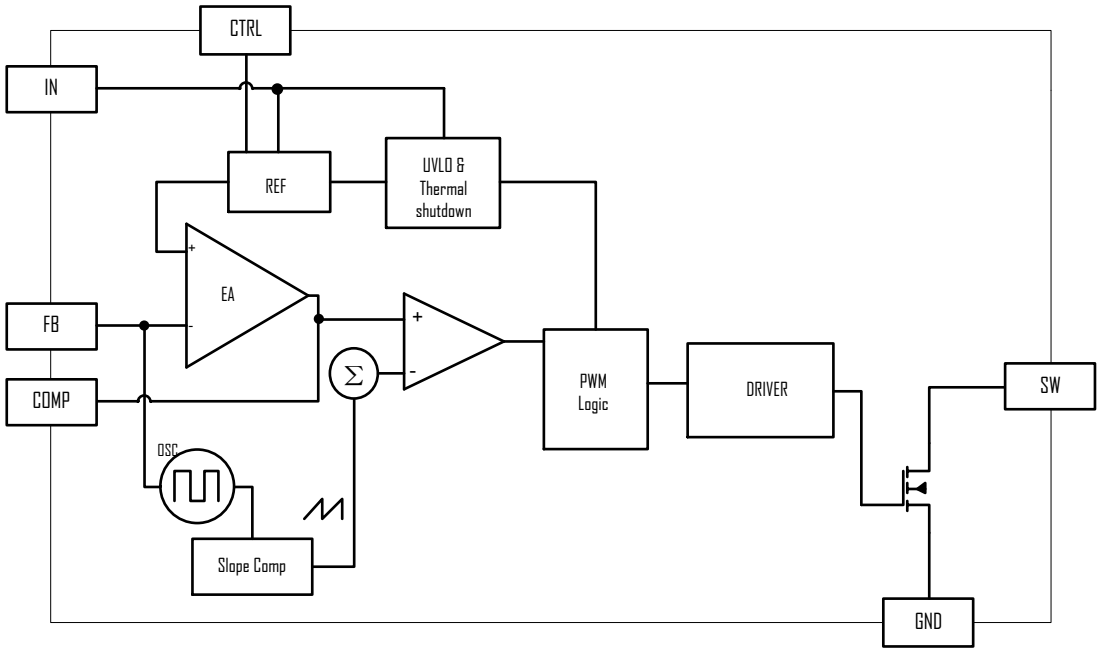
Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability.
The output requires a capacitor in the range of 0.47μF to 10μF. If smaller output cap is used, a larger compensation cap will be needed. For example, if a 0.47uF output cap is used, the compensation cap has to be 470nF for loop stability. The capacitor in the range of 1μF to 4.7μF is recommended for input side.

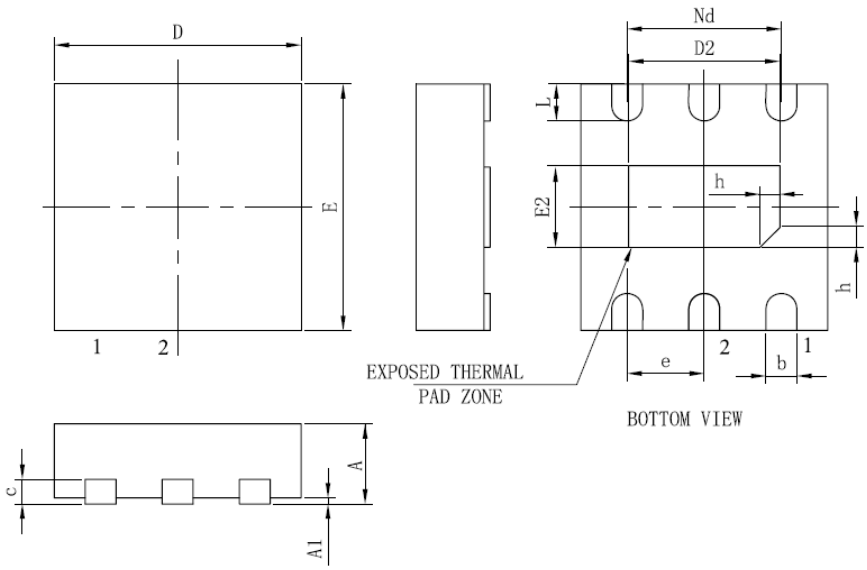
PCB Layout



BLOCK DIAGRAM



PACKAGE OUTLINE



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	1.95	2.00	2.05
D2	1.00	—	1.45
e	0.65BSC		
Nd	1.30BSC		
E	1.95	2.00	2.05
E2	0.50	--	0.85
L	0.25	0.30	0.40
h	0.10	0.15	0.20